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Kind regards,

Team Nexperia

DATA SHEET

74F373

Octal transparent latch (3-State)

74F374

Octal D flip-flop (3-State)

Product data
Supersedes data of 1994 Dec 05

2002 Nov 20

Latch/flip-flop

74F373/74F374

74F373 Octal transparent latch (3-State)
74F374 Octal D-type flip-flop (3-State)

FEATURES

- 8-bit transparent latch — 74F373
- 8-bit positive edge triggered register — 74F374
- 3-State outputs glitch free during power-up and power-down
- Common 3-State output register
- Independent register and 3-State buffer operation
- SSOP Type II Package

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable (\overline{OE}) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is HIGH. The latch remains transparent to the data input while E is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW output enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation. When \overline{OE} is LOW, latched or transparent data appears at the output.

When \overline{OE} is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F374 is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of the D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW output enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|---------------------------|--------------------------------|
| 74F373 | 4.5 ns | 35 mA |

| TYPE | TYPICAL f_{\max} | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|--------------------|--------------------------------|
| 74F374 | 165 MHz | 55 mA |

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | PKG DWG # |
|-----------------------------|---|-----------|
| | COMMERCIAL RANGE $V_{CC} = 5\text{ V} \pm 10\%$, $T_{\text{amb}} = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$ | |
| 20-pin plastic DIP | N74F373N, N74F374N | SOT146-1 |
| 20-pin plastic SOL | N74F373D, N74F374D | SOT163-1 |
| 20-pin plastic SSOP type II | N74F373DB, N74F374DB | SOT339-1 |

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

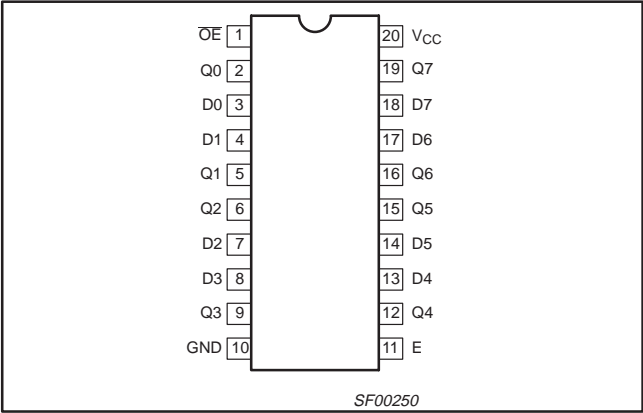
| PINS | DESCRIPTION | 74F (U.L.) HIGH / LOW | LOAD VALUE HIGH/LOW |
|-----------------|--|-----------------------|---------------------------|
| D0 - D7 | Data inputs | 1.0 / 1.0 | 20 μA / 0.6 mA |
| E (74F373) | Enable input (active-HIGH) | 1.0 / 1.0 | 20 μA / 0.6 mA |
| \overline{OE} | Output enable inputs (active-LOW) | 1.0 / 1.0 | 20 μA / 0.6 mA |
| CP (74F374) | Clock pulse input (active rising edge) | 1.0 / 1.0 | 20 μA / 0.6 mA |
| Q0 - Q7 | 3-State outputs | 150 / 40 | 3.0 mA / 24 mA |

NOTE: One (1.0) FAST unit load is defined as: 20 μA in the HIGH state and 0.6 mA in the LOW state.

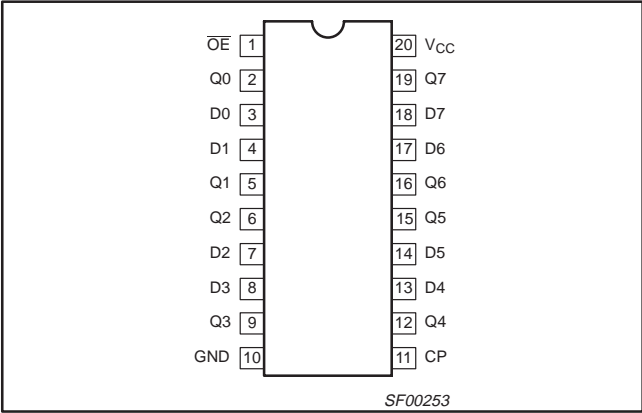
Latch/flip-flop

74F373/74F374

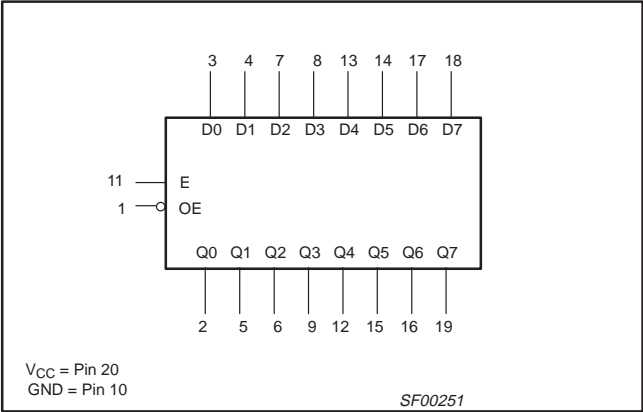
PIN CONFIGURATION – 74F373



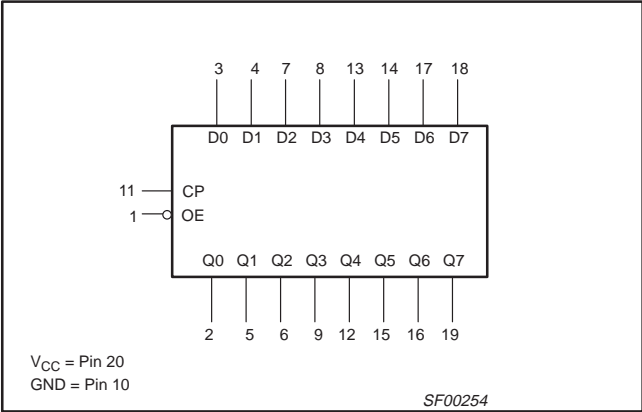
PIN CONFIGURATION – 74F374



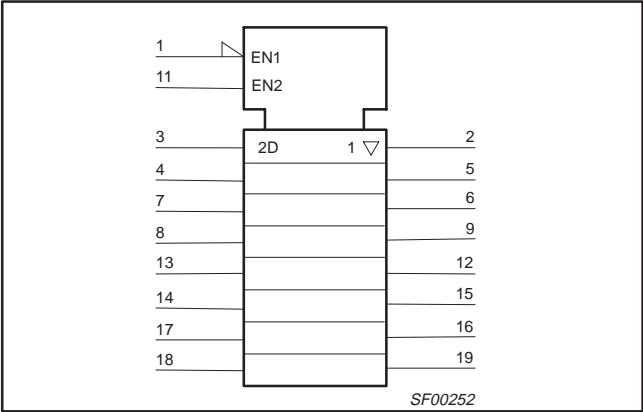
LOGIC SYMBOL – 74F373



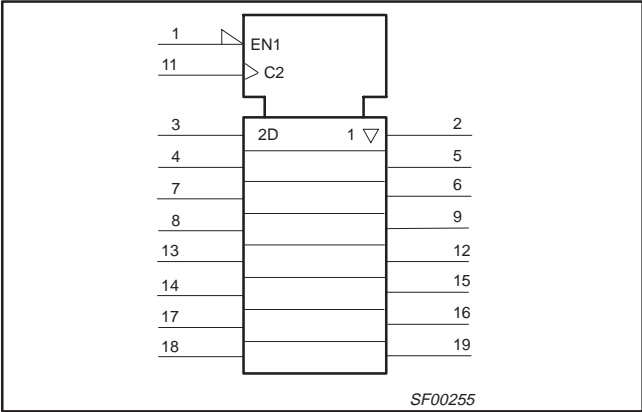
IEC/IEE SYMBOL – 74F374



IEC/IEEE SYMBOL – 74F373



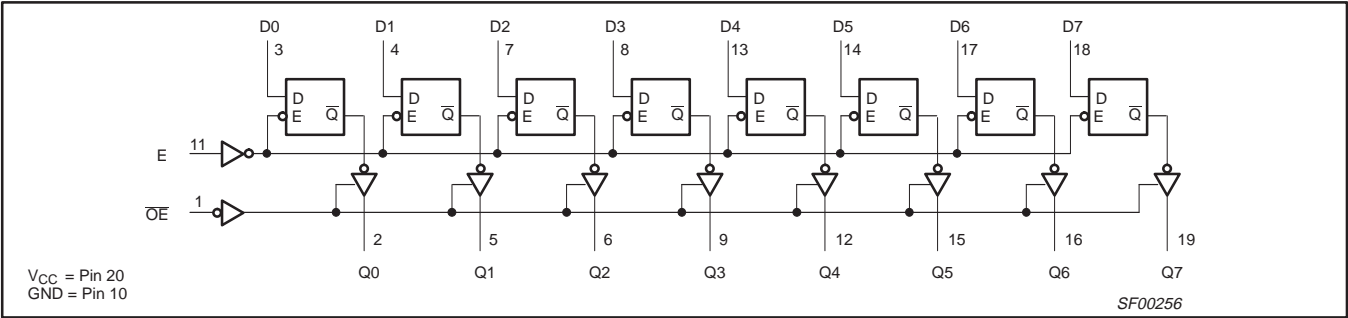
IEC/IEEE SYMBOL – 74F374



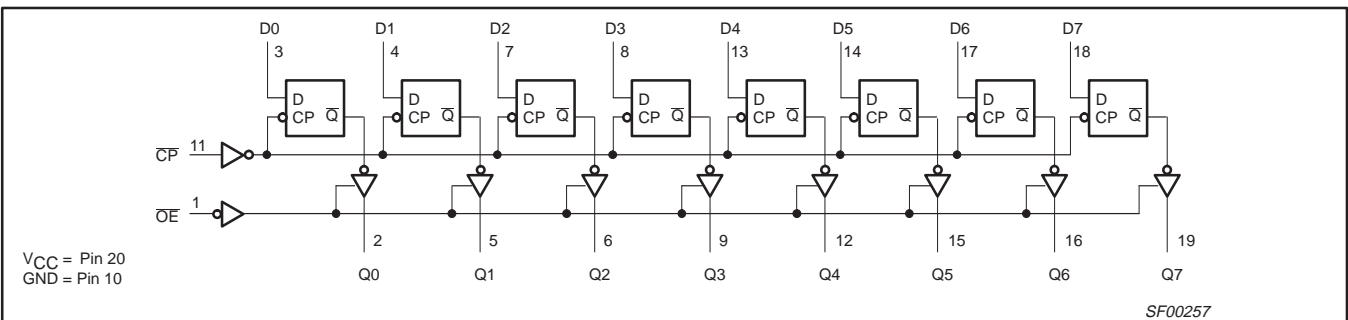
Latch/flip-flop

74F373/74F374

LOGIC DIAGRAM FOR 74F373



LOGIC DIAGRAM FOR 74F374



FUNCTION TABLE FOR 74F373

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODE |
|--------|---|----|-------------------|---------|--------------------------|
| OE | E | Dn | | Q0 - Q7 | |
| L | H | L | L | L | Enable and read register |
| L | H | H | H | H | |
| L | ↓ | l | L | L | Latch and read register |
| L | ↓ | h | H | H | |
| L | L | X | NC | NC | Hold |
| H | L | X | NC | Z | Disable outputs |
| H | H | Dn | Dn | Z | |

NOTES:
H = High-voltage level
h = HIGH state must be present one set-up time before the HIGH-to-LOW enable transition
L = Low-voltage level
l = LOW state must be present one set-up time before the HIGH-to-LOW enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = HIGH-to-LOW enable transition

Latch/flip-flop

74F373/74F374

FUNCTION TABLE FOR 74F374

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODE |
|-----------------|------------|----|-------------------|---------|------------------------|
| \overline{OE} | CP | Dn | | Q0 – Q7 | |
| L | \uparrow | l | L | L | Load and read register |
| L | \uparrow | h | H | H | |
| L | \uparrow | X | NC | NC | Hold |
| H | \uparrow | X | NC | Z | Disable outputs |
| H | \uparrow | Dn | Dn | Z | |

NOTES:

H = High-voltage level

h = HIGH state must be present one set-up time before the LOW-to-HIGH clock transition

L = Low-voltage level

l = LOW state must be present one set-up time before the LOW-to-HIGH clock transition

NC= No change

X = Don't care

Z = High impedance "off" state

 \uparrow = LOW-to-HIGH clock transition \uparrow = Not LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limit set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free air temperature range.

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|-------------------------|------|
| V _{CC} | Supply voltage | –0.5 to +7.0 | V |
| V _{IN} | Input voltage | –0.5 to +7.0 | V |
| I _{IN} | Input current | –30 to +5 | mA |
| V _{OUT} | Voltage applied to output in HIGH output state | –0.5 to V _{CC} | V |
| I _{OUT} | Current applied to output in LOW output state | 48 | mA |
| T _{amb} | Operating free air temperature range | 0 to +70 | °C |
| T _{stg} | Storage temperature range | –65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | HIGH-level input voltage | 2.0 | – | – | V |
| V _{IL} | LOW-level input voltage | – | – | 0.8 | V |
| I _{Ik} | Input clamp current | – | – | –18 | mA |
| I _{OH} | HIGH-level output current | – | – | –3 | mA |
| I _{OL} | LOW-level output current | – | – | 24 | mA |
| T _{amb} | Operating free air temperature range | 0 | – | +70 | °C |

Latch/flip-flop

74F373/74F374

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|------------------|--|--------|---|---------------------|--------------------|-------|------|------|
| | | | | MIN | TYP ² | MAX | | |
| V _{OH} | HIGH-level output voltage | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX | ±10%V _{CC} | 2.4 | | V | |
| | | | | ±5%V _{CC} | 2.7 | 3.4 | | V |
| V _{OL} | LOW-level output voltage | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX | ±10%V _{CC} | | 0.35 | 0.50 | V |
| | | | | | ±5%V _{CC} | | 0.35 | 0.50 |
| V _{IK} | Input clamp voltage | | V _{CC} = MIN, I _I = I _{IK} | | | −0.73 | −1.2 | V |
| I _I | Input current at maximum input voltage | | V _{CC} = MAX, V _I = 7.0 V | | | | 100 | μA |
| I _{IH} | High-level input current | | V _{CC} = MAX, V _I = 2.7 V | | | | 20 | μA |
| I _{IL} | Low-level input current | | V _{CC} = MAX, V _I = 0.5 V | | | | −0.6 | mA |
| I _{OZH} | Off-state output current, high-level voltage applied | | V _{CC} = MAX, V _O = 2.7 V | | | | 50 | μA |
| I _{OZL} | Off-state output current, low-level voltage applied | | V _{CC} = MAX, V _O = 0.5 V | | | | −50 | μA |
| I _{OS} | Short-circuit output current ³ | | V _{CC} = MAX | −60 | | | −150 | mA |
| I _{CC} | Supply current (total) | 74F373 | V _{CC} = MAX | | | 35 | 60 | mA |
| | | 74F374 | | | | 57 | 86 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | TEST CONDITION | LIMITS | | | | | UNIT |
|--------------------------------------|---|--------|--------------------------|---|------------|-------------|---|-------------|------|
| | | | | T _{amb} = +25 °C V _{CC} = +5.0 V C _L = 50 pF; R _L = 500 Ω | | | T _{amb} = 0 °C to +70 °C V _{CC} = +5.0 V ± 10% C _L = 50 pF; R _L = 500 Ω | | |
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{PLH} t _{PHL} | Propagation delay Dn to Qn | 74F373 | Waveform 3 | 3.0 2.0 | 5.3 3.7 | 7.0 5.0 | 3.0 2.0 | 8.0 6.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay E to Qn | | Waveform 2 | 5.0 3.0 | 9.0 4.0 | 11.5 7.0 | 5.0 3.0 | 12.0 8.0 | ns |
| t _{PZH} t _{PZL} | Output enable time to HIGH or LOW level | | Waveform 6 Waveform 7 | 2.0 2.0 | 5.0 5.6 | 11.0 7.5 | 2.0 2.0 | 11.5 8.5 | ns |
| t _{PHZ} t _{PLZ} | Output disable time from HIGH or LOW level | | Waveform 6 Waveform 7 | 2.0 2.0 | 4.5 3.8 | 6.5 5.0 | 2.0 2.0 | 7.0 6.0 | ns |
| f _{max} | Maximum clock frequency | 74F374 | Waveform 1 | 150 | 165 | | 140 | | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to Qn | | Waveform 1 | 3.5 3.5 | 5.0 5.0 | 7.5 7.5 | 3.0 3.0 | 8.5 8.5 | ns |
| t _{PZH} t _{PZL} | Output enable time to HIGH or LOW level | | Waveform 6 Waveform 7 | 2.0 2.0 | 9.0 5.3 | 11.0 7.5 | 2.0 2.0 | 12.0 8.5 | ns |
| t _{PHZ} t _{PLZ} | Output disable time from HIGH or LOW level | | Waveform 6 Waveform 7 | 2.0 2.0 | 5.3 4.3 | 6.0 5.5 | 2.0 2.0 | 7.0 6.5 | ns |

Latch/flip-flop

74F373/74F374

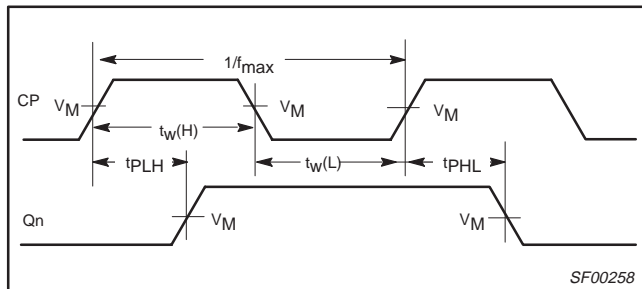
AC SET-UP REQUIREMENTS

| SYMBOL | PARAMETER | | TEST CONDITION | LIMITS | | | | | UNIT |
|--|--|--------|-------------------|---|-----|-----|---|-----|------|
| | | | | T _{amb} = +25 °C V _{CC} = +5.0 V C _L = 50 pF, R _L = 500 Ω | | | T _{amb} = 0 °C to +70 °C V _{CC} = +5.0 V ± 10% C _L = 50 pF, R _L = 500 Ω | | |
| | | | | MIN | TYP | MAX | MIN | MAX | |
| | | | | | | | | | |
| t _{su} (H) t _{su} (L) | Set-up time, HIGH or LOW level Dn to E | 74F373 | Waveform 4 | 0 1.0 | | | 0 1.0 | | ns |
| t _h (H) t _h (L) | Hold time, HIGH or LOW level Dn to E | | Waveform 4 | 3.0 3.0 | | | 3.0 3.0 | | ns |
| t _w (H) | E Pulse width, HIGH | | Waveform 1 | 3.5 | | | 4.0 | | ns |
| t _{su} (H) t _{su} (L) | Set-up time, HIGH or LOW level Dn to CP | 74F374 | Waveform 5 | 2.0 2.0 | | | 2.0 2.0 | | ns |
| t _h (H) t _h (L) | Hold time, HIGH or LOW level Dn to CP | | Waveform 5 | 0 0 | | | 0 0 | | ns |
| t _w (H) t _w (L) | CP Pulse width, HIGH or LOW | | Waveform 5 | 3.5 4.0 | | | 3.5 4.0 | | ns |

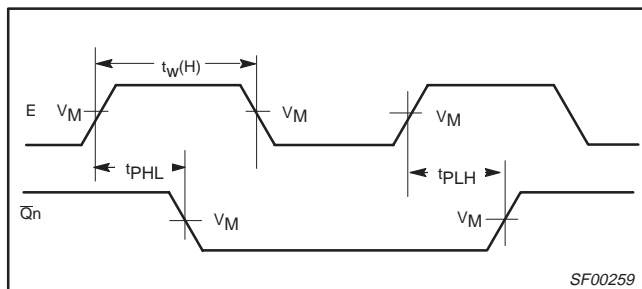
AC WAVEFORMS

For all waveforms, $V_M = 1.5\text{ V}$.

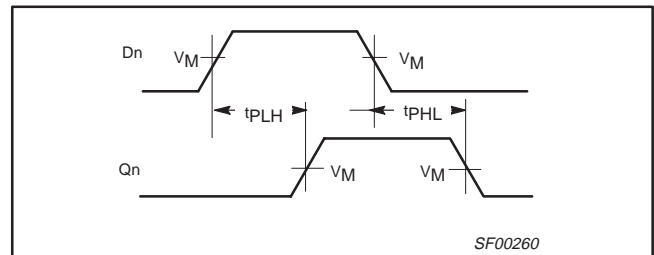
The shaded areas indicate when the input is permitted to change for predictable output performance.



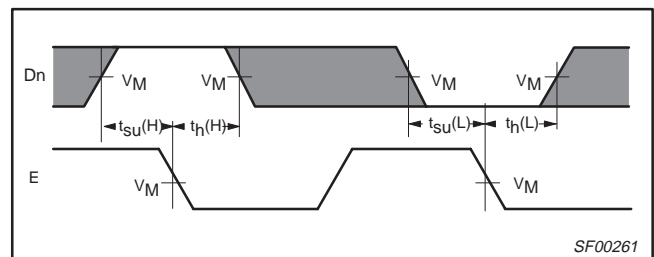
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 2. Propagation delay for enable to output and enable pulse width



Waveform 3. Propagation delay for data to output



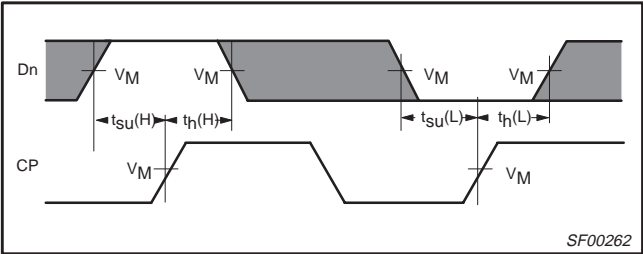
Waveform 4. Data set-up time and hold times

Latch/flip-flop

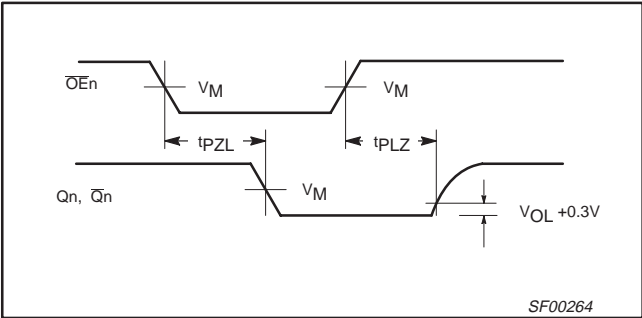
74F373/74F374

AC WAVEFORMS *(continued)*

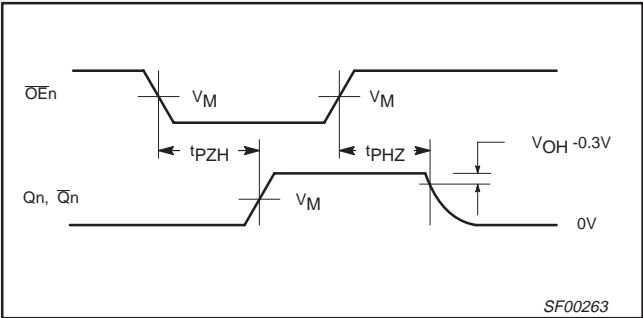
For all waveforms, $V_M = 1.5\text{ V}$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 5. Data set-up time and hold times



Waveform 7. 3-State output enable time to LOW level and output disable time from LOW level



Waveform 6. 3-State output enable time to HIGH level and output disable time from HIGH level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

| TEST | SWITCH |
|-----------------------|--------|
| t_{PLZ} , t_{PZL} | closed |
| All other | open |

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

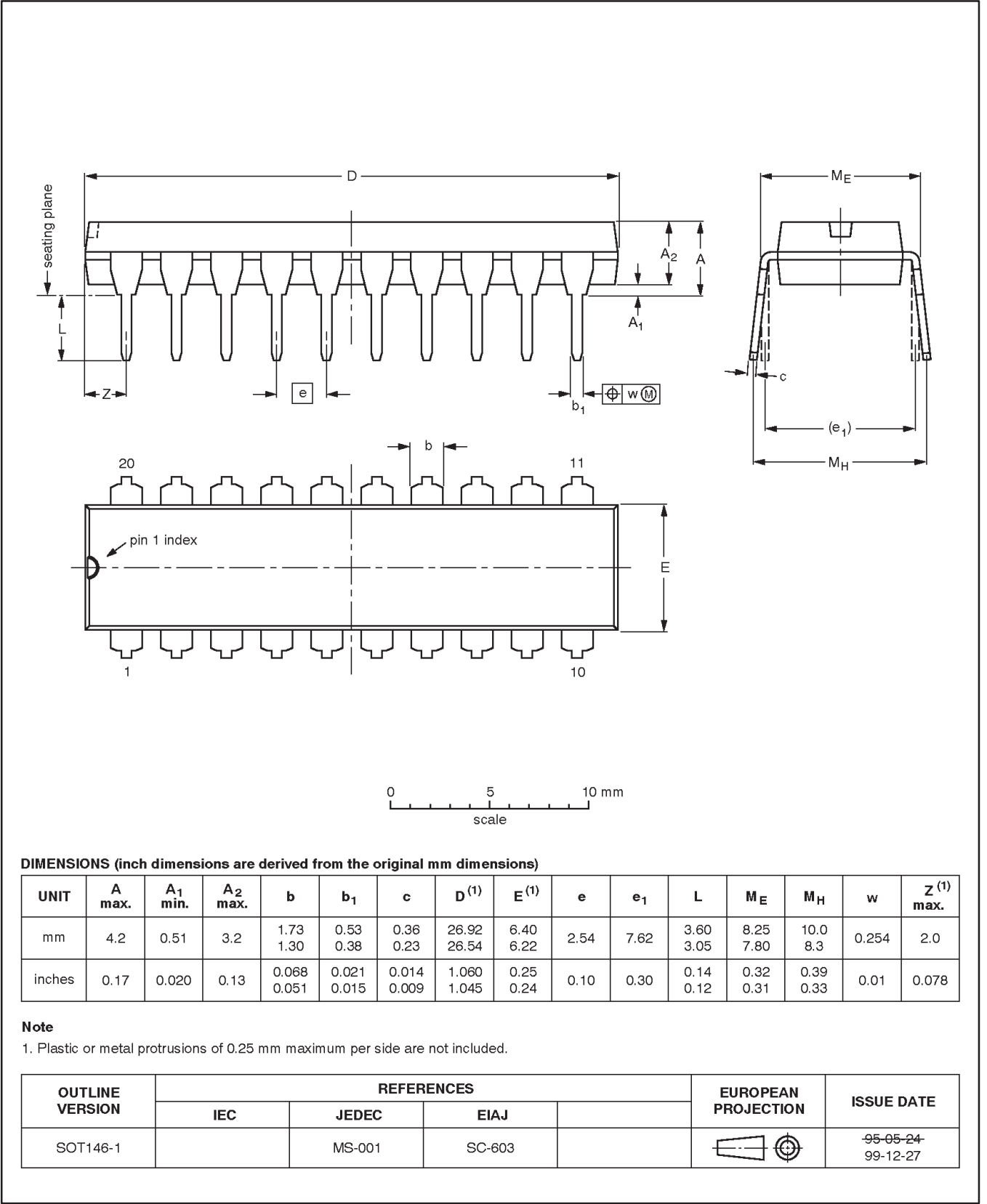
SF00265

Latch/flip-flop

74F373/74F374

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

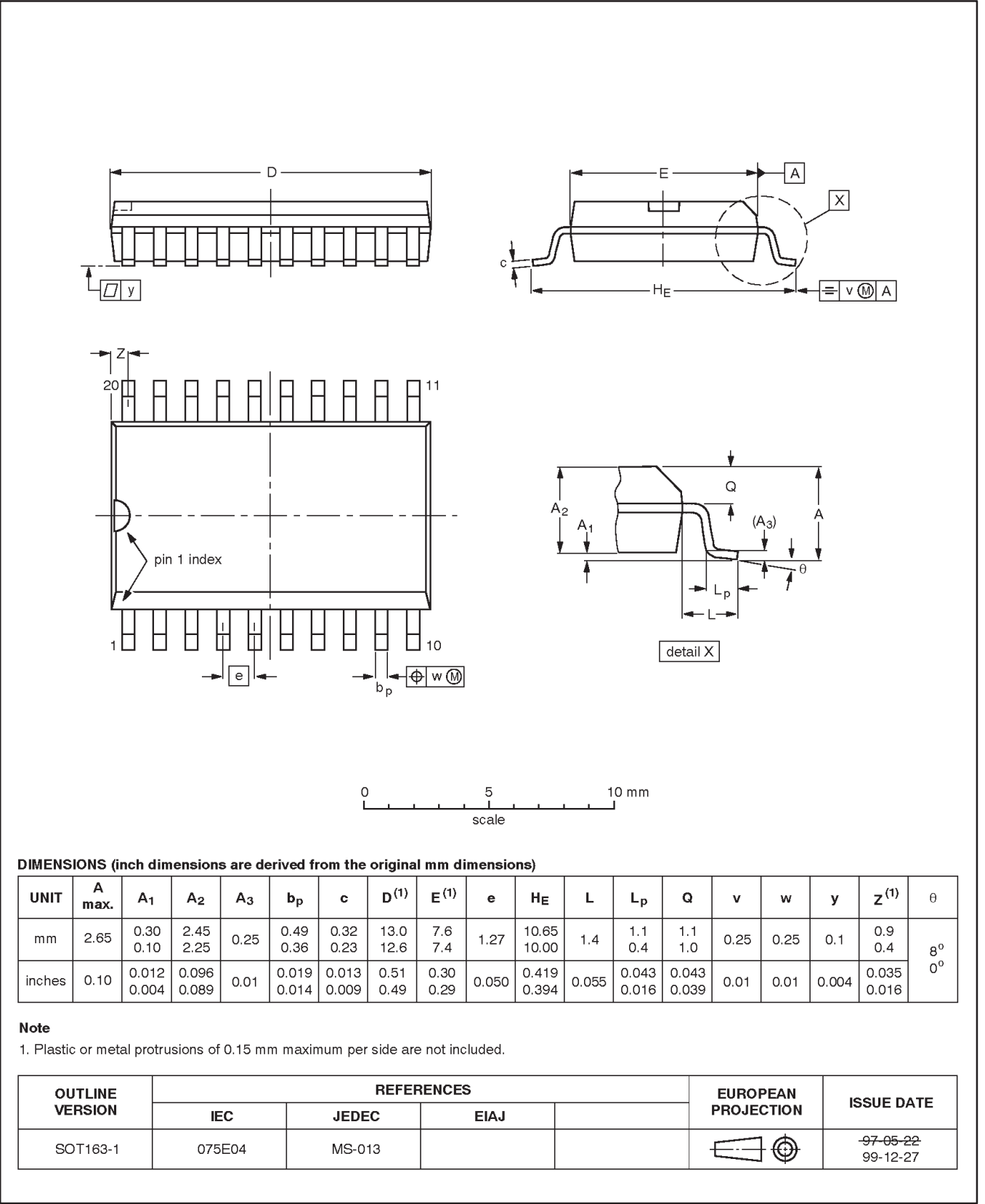


Latch/flip-flop

74F373/74F374

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

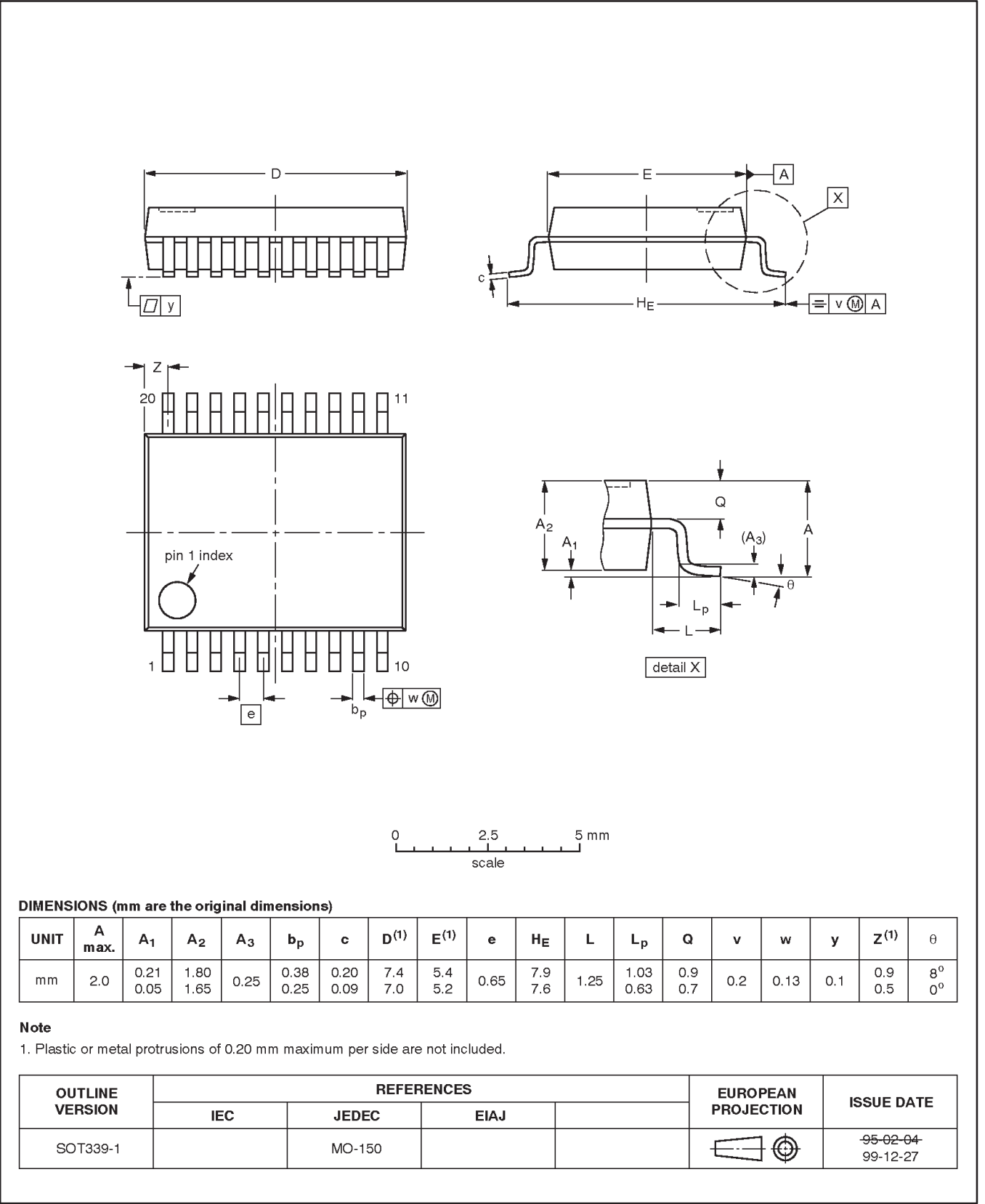


Latch/flip-flop

74F373/74F374

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



Latch/flip-flop

74F373/74F374

REVISION HISTORY

| Rev | Date | Description |
|-----|----------|--|
| _3 | 20021120 | Product data; third version (9397 750 10758). Supersedes 74F373_374_2 dated 1994 Dec 05 (9397 750 05119). Engineering Change Notice 853–0369 29206 (date: 20021115). Modifications: <ul style="list-style-type: none">• Corrected ordering information table (from 'N74374DB' to '74F374DB').• Add SSOP20 (SOT339-1) package outline drawing. |
| _2 | 19941205 | Product data; second version (9397 750 05119). Engineering Change Notice 853–0369 14383 (date: 19941205). |

Latch/flip-flop

74F373/74F374

Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2] [3]} | Definitions |
|-------|----------------------------------|-----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 11-02

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Document order number: 9397 750 10758

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