Dual Precision JFET-Input Operational Amplifier

OP215

FEATURES
High Slew Rate: 10 V/μs Min
Fast Settling Time: 0.9 μs to 0.1% Type
Low Input Offset Voltage Drift: 10 μV/°C Max
Wide Bandwidth: 3.5 MHz Min
Temperature-Compensated Input Bias Currents
Guaranteed Input Bias Current: 18 nA Max (125°C)
Bias Current Specified Warmed Up over Temperature
Low Input Noise Current: 0.01 pA/√Hz Type
High Common-Mode Rejection Ratio 86 dB Min
Pin Compatible with Standard Dual Pinouts
Models with MIL-STD-883 Class B Processing Available

GENERAL DESCRIPTION

The OP215 offers the proven JFET-input performance advantages of high speed and low input bias current with the tracking and convenience advantages of a dual op amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.

On-chip zener-zap trimming is used to achieve low V_{OS}, while a bias-current compensation scheme gives a low input bias current at elevated temperature. Thus, the OP215 features an input bias current of 1.4 nA at 70°C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP249 and AD712 data sheets.

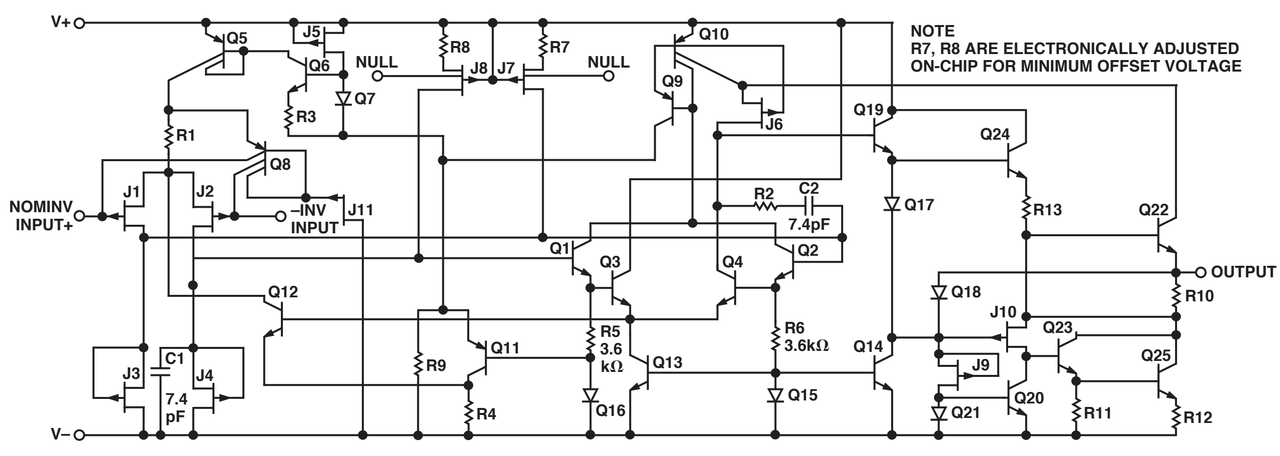

Figure 1. Simplified Schematic (1/2 OP215)

REV. A

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OP215–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP215E Min	OP215E Type	OP215E Max	OP215G Min	OP215G Type	OP215G Max	Unit
Input Offset Voltage	V_{OS}	R_S = 50 Ω 'G' Grade		0.2	1.0		2.0 2.5	4.0 6.0	mV mV
Input Offset Current[1]	I_{OS}	T_j = 25°C Device Operating		3 5	50 100		3 5	100 200	pA pA
Input Bias Current[1]	I_B	T_j = 25°C Device Operating		±15 ±18	±100 ±300		±15 ±18	±300 ±600	pA pA
Input Resistance	R_{IN}			$10^{1,2}$			$10^{1,2}$		Ω
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	150	500		50	200		V/mV
Output Voltage Swing	V_O	R_L = 10 kΩ R_L = 2 kΩ	±12 ±11	±13 ±12.7		±12 ±11	±13 ±12.7		V V
Supply Current	I_{SY}	 'G' Grade		6.0	8.5		7.0 7.0	10.0 12.0	mA mA
Slew Rate	SR	A_{VCL} = 1	10	18		5	15		V/μs
Gain Bandwidth Product[3]	GBW		3.5	5.7		3.0	5.4		MHz
Closed-Loop Bandwidth	CLBW	A_{VCL} = 1		13			12		MHz
Setting Time	t_S	To 0.01% To 0.05%[2] To 0.10%		2.3 1.1 0.9			2.4 1.2 1.0		μs μs μs
Input Voltage Range	IVR		10.2 –10.2	14.8 –11.5		10.1 –10.1	14.8 –11.5		V V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±IVR E, G Grades	82	100		80	96		dB
Power Supply Rejection Ratio	PSRR	V_S = ±10 V to ±16 V V_S = ±10 V to ±15 V		10	51		 16	 100	μV/V μV/V
Input Noise Voltage Density	θn	f_O = 100 Hz f_O = 1,000 Hz		20 15			20 15		nV/√Hz nV/√Hz
Input Noise Current Density	I_n	f_O = 100 Hz f_O = 1,000 Hz		0.01 0.01			0.01 0.01		pA/√Hz pA/√Hz
Input Capacitance	C_{IN}			3			3		pF

NOTES

[1]Input bias current is specified for two different conditions. The T_j = 25°C specification is with the junction at ambient temperature; the device operating specification is with the device operating in a warmed up condition at 25°C ambient. The warmed up bias-current value is correlated to the junction temperature value via the curves of I_S versus T_j and I_S versus T_A. PMI has a bias-current compensation circuit that gives improved bias current and bias current over temperature versus standard JFET input op amps. I_S and I_{OS} are measured at V_{CM} = 0.

[2]Setting time is defined here for a unity gain inverter connection using 2 kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10 V step input is applied to the inverter. See setting time test circuit.

[3]Sample tested.

Specifications are subject to change without notice.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, 0°C ≤ T_A ≤ 70°C for E Grade, –40°C ≤ T_A ≤ +85°C for G Grade, unless otherwise noted.)

Parameter	Symbol	Conditions	OP215E Min	OP215E Type	OP215E Max	OP215G Min	OP215G Type	OP215G Max	Unit
Input Offset Voltage	V_{OS}	R_S = 50 Ω		0.4	1.65		3.5	8.0	mV
Average Input Offset Voltage Drift									
Without External Trim[1]	TCV_{OS}			3	15		6		µV/°C
With External Trim	TCV_{OSn}	R_P = 100 kΩ		3			4		µV/°C
Input Offset Current[2]	I_{OS}	T_j = 70°C		0.06	0.45		0.08	0.65	nA
		T_A = 70°C Device Operating		0.08	0.80		0.10	1.2	nA
Input Bias Current[2]	I_S	T_j = 70°C		±0.12	±0.70		±0.14	±0.9	nA
		T_A = 70°C Device Operating		±0.16	±1.40		±0.19	±1.8	nA
Input Voltage Range	IVR		10.2	14.7		10.1	14.7		V
			–10.2	–11.4		–10.1	–11.3		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±IVR	80	98		76	94		dB
Power Supply Rejection Ratio	PSRR	V_S = ±10 V to ±16 V		13	100				
		V_S = ±10 V to ±15 V					20	159	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	50	180		35	130		V/mV
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12	±13		±12	±13		V

NOTES
[1]Sample tested.
[2]Input bias current is specified for two different conditions. The T_j = 25°C specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed up condition at 25°C ambient. The warmed up bias-current value is correlated to the junction temperature value via the curves of I_S versus T_j and I_S versus T_A. PMI has a bias-current compensation circuit that gives improved bias current and bias current over temperature versus standard JFET input op amps. I_S and I_{OS} are measured at V_{CM} = 0.
Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

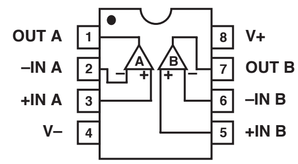
Supply Voltage
OP215E, OP215G . . . . ±18 V
Operating Temperature Range
OP215E . . . . +0°C to +70°C
OP215G . . . . –40°C to +85°C
Maximum Junction Temperature (T_j) . . . . 150°C
Differential Input Voltage
OP215E . . . . ±40 V
OP215G . . . . ±30 V
Input Voltage[2]
OP215E . . . . ±20 V
OP215G . . . . ±16 V
Output Short-Circuit Duration . . . . Indefinite
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . 300°C
Junction Temperature (T_j) . . . . –65°C to +150°C

NOTES
[1]Absolute maximum ratings apply to packaged parts, unless otherwise noted.
[2]Unless otherwise specified, the absolute maximum negative input voltage is equal to one volt more positive than the negative power supply voltage.

Package Type	θ_{JA} *	θ_{JC}	Unit
8-Lead Hermetic DIP (Z)	134	12	°C/W
8-Lead Plastic DIP (P)	96	37	°C/W

*θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

PIN CONFIGURATION



ORDERING INFORMATION[1]

Model	Package Type	Temperature Range	T_A = 25°C, V_{OS} Max (mV)
OP215EZ[2]	8-Lead CerDIP	COM	1.0
OP215GP[2]	8-Lead Plastic DIP	XIND	6.0

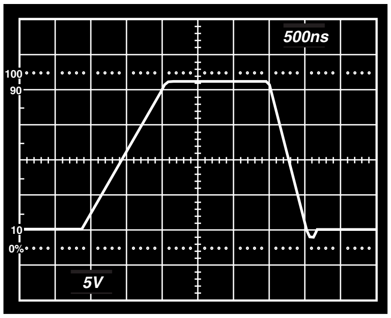
For military processed devices, please refer to the standard microcircuit drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
5962-8853801GA[2]	OP215AJMDA
5962-8853801PA	OP215AZMDA
5962-8838032A[2]	OP215BRCMDA

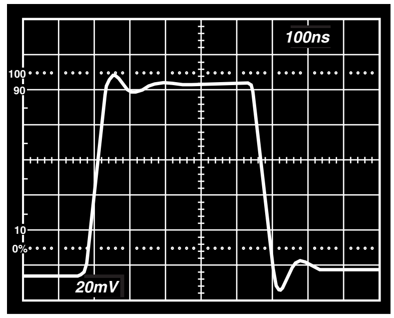
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.
[2]Not for new design, obsolete April 2002.

CAUTION

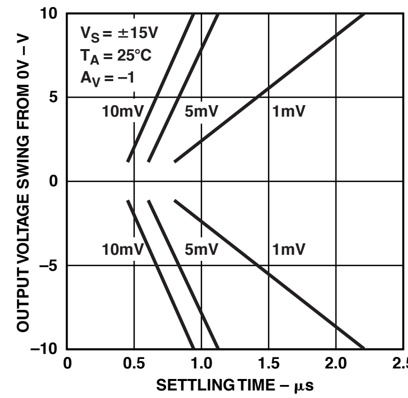
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP215 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



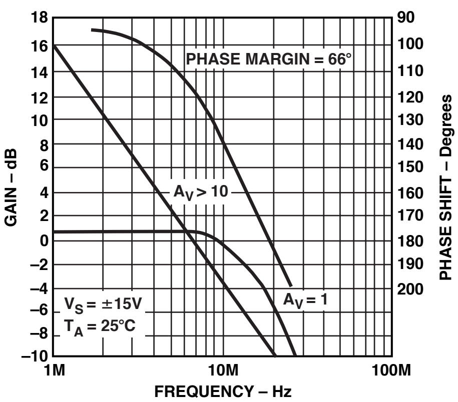
TPC 1. Large-Signal Transient Response



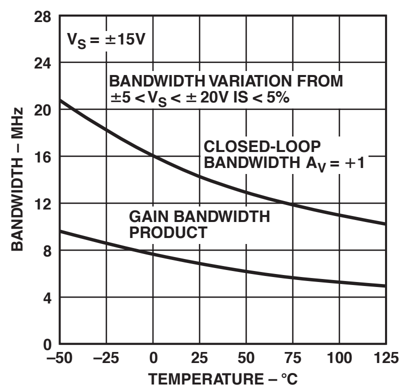
TPC 2. Small-Signal Transient Response



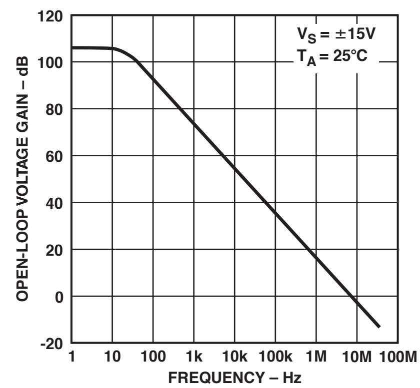
TPC 3. Settling Time



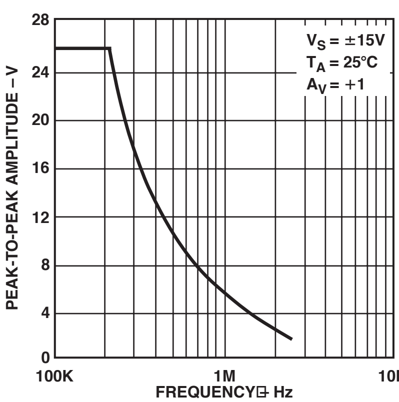
TPC 4. Closed-Loop Bandwidth and Phase Shift vs. Frequency



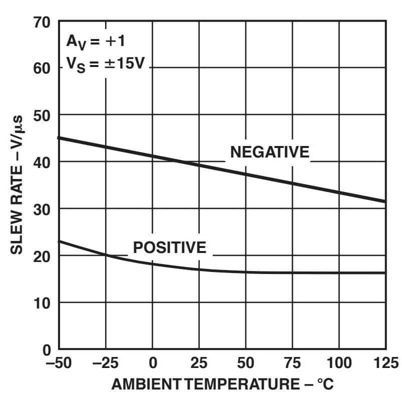
TPC 5. Bandwidth vs. Temperature



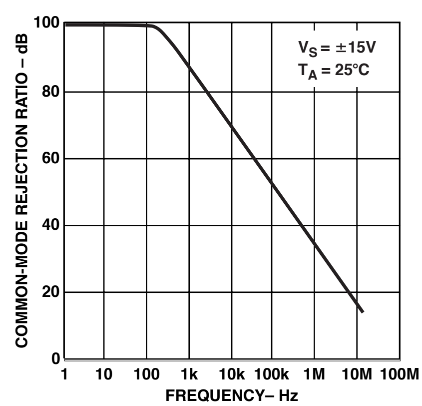
TPC 6. Open-Loop Frequency Response



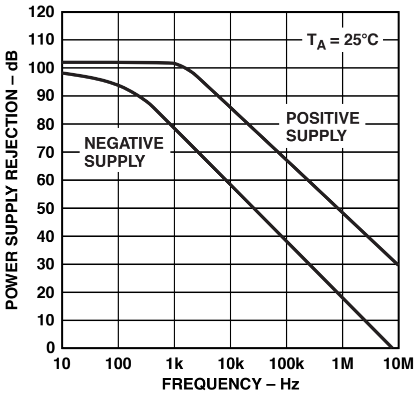
TPC 7. Maximum Output Swing vs. Frequency



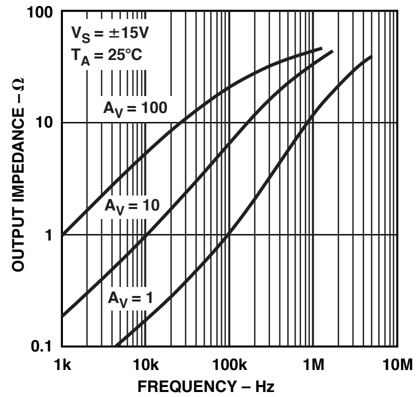
TPC 8. Slew Rate vs. Temperature



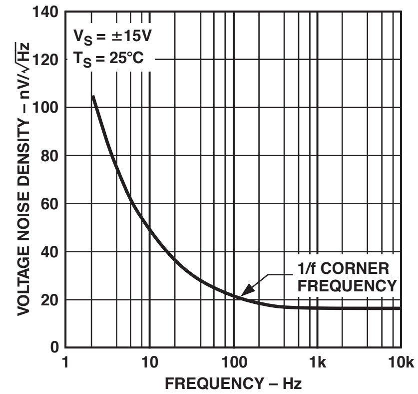
TPC 9. Common-Mode Rejection Ratio vs. Frequency



TPC 10. Power Supply Rejection vs. Frequency



TPC 11. Output Impedance vs. Frequency



TPC 12. Voltage Noise Density vs. Frequency

BASIC CONNECTIONS

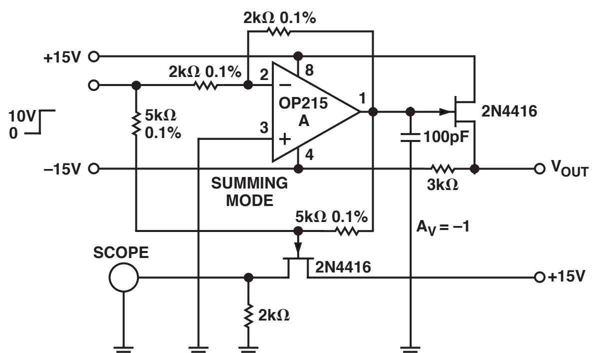
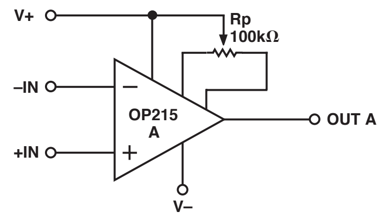


Figure 2. Settling Time Test Circuit



NOTE
V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10 kΩ TO 1 MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

Figure 4. Input Offset Voltage Nulling

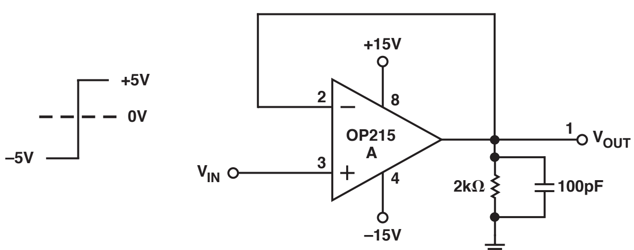


Figure 3. Slew Rate Test Circuit

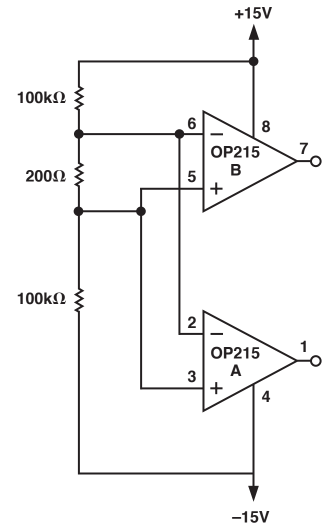
APPLICATIONS INFORMATION

Dynamic Operating Considerations

As with most amplifiers, care should be taken with lead dress, component placement, and supply de-coupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3 dB frequency of the closed-loop gain and, consequently, there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.

BASIC CONNECTIONS



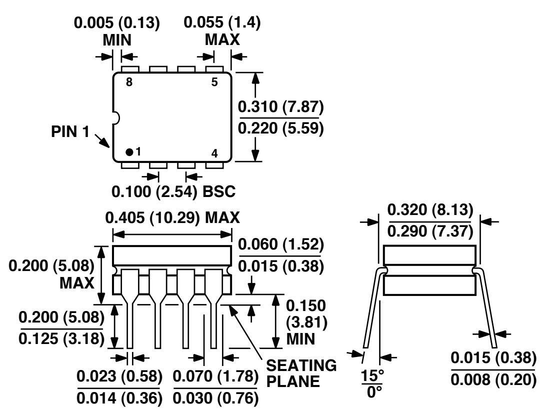
NOTES
1. T_A = 125°C TO 150°C
2. RESISTORS ARE TYPE RN55D, ± 1%

Figure 5. Burn-In Circuit

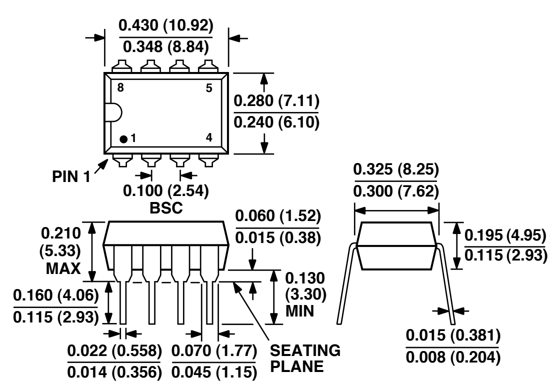
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead CERDIP (Z-Suffix)



8-Lead Plastic DIP (P-Suffix)



Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Edits to GENERAL DESCRIPTION	1
Edits to ELECTRICAL CHARACTERISTICS	2, 3
Edits to ORDERING INFORMATION	4
Edits to PIN CONNECTIONS	4
Edits to ABSOLUTE MAXIMUM RATINGS	4
Edits to PACKAGE TYPE	4
Deleted WAFER TEST LIMITS	4
Deleted DICE CHARACTERISTICS	4
Deleted TYPICAL ELECTRICAL CHARACTERISTICS	4
Edits to BURN-IN CIRCUIT figure	7

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