EiceDRIVER™ 1ED38x0Mc12M Enhanced

Datasheet

Single-channel 5.7 kV (rms) isolated gate driver IC with I2C configurability for DESAT, Soft-off, UVLO, Miller clamp and optional two-level turn-off

Features

- 650 V, 1200 V, 1700 V, 2300 V IGBTs, SiC, and Si MOSFETs
- 40 V absolute maximum output supply voltage
- ±3 A, ±6 A, and ±9 A typical sinking and sourcing peak output current
- Separate source and sink outputs for hard switching or optional two-level turn-off and with active Miller clamp
- I2C bus for parameter configuration and status register readout
- Precise, adjustable, and temperature compensated V_{CEsat} detection (DESAT) with fault output
- Adjustable IGBT soft turn-off after desaturation detection
- Operation at high ambient temperature up to 125 °C with over-temperature shut down at 160 °C (±10 °C)
- Tight IC-to-IC propagation delay matching ($t_{PDD,max}$ = 30 ns)
- Undervoltage lockout protection with hysteresis for input and output side with active shut-down
- Configurable feedback or fault-off behavior for comparator result of integrated ADC
- High common-mode transient immunity CMTI = 200 kV/µs
- Small space-saving DSO-16 fine-pitch package with large creepage distance (>8 mm)
- Safety certification
  - UL 1577 recognized (File E311313) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
  - IEC 60747-17/VDE 0884-11 approval (pending) with V_{IORM} = 1767 V (peak, reinforced)
- Additional ***reference manual*** available for detailed functional description

Potential applications

- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters
- UPS systems
- Welding
- Commercial and agricultural vehicles (CAV)
- Commercial air-conditioning (CAC)
- High-voltage isolated DC-DC converters
- Isolated switch mode power supplies (SMPS)

PG-DSO-16

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

Product type	Output current	Isolation class	Marking	OPN
1ED3830MC12M	3 A (typ)	reinforced	3830MC12	***1ED3830MC12MXUMA1***
1ED3860MC12M	6 A (typ)	reinforced	3860MC12	***1ED3860MC12MXUMA1***
1ED3890MC12M	9 A (typ)	reinforced	3890MC12	***1ED3890MC12MXUMA1***
1ED3830MU12M	3 A (typ)	UL 1577	3830MU12	***1ED3830MU12MXUMA1***
1ED3860MU12M	6 A (typ)	UL 1577	3860MU12	***1ED3860MU12MXUMA1***
1ED3890MU12M	9 A (typ)	UL 1577	3890MU12	***1ED3890MU12MXUMA1***

Description

The 1ED38x0Mc12M family (X3 Digital) consists of galvanically isolated single channel gate driver ICs in a small PG-DSO-16 package with a large creepage and clearance of 8 mm. The gate driver ICs provide a typical peak output current of 3 A, 6 A, and 9 A.

Adjustable control and protection functions are included to simplify the design of highly reliable systems. All parameter adjustments are done from the input side via the I2C interface (pin SDA and SCL).

All logic I/O pins are supply voltage dependent 3.3 V or 5 V CMOS compatible and can be directly connected to a microcontroller.

The data transfer across the galvanic isolation is realized by the integrated coreless transformer technology.

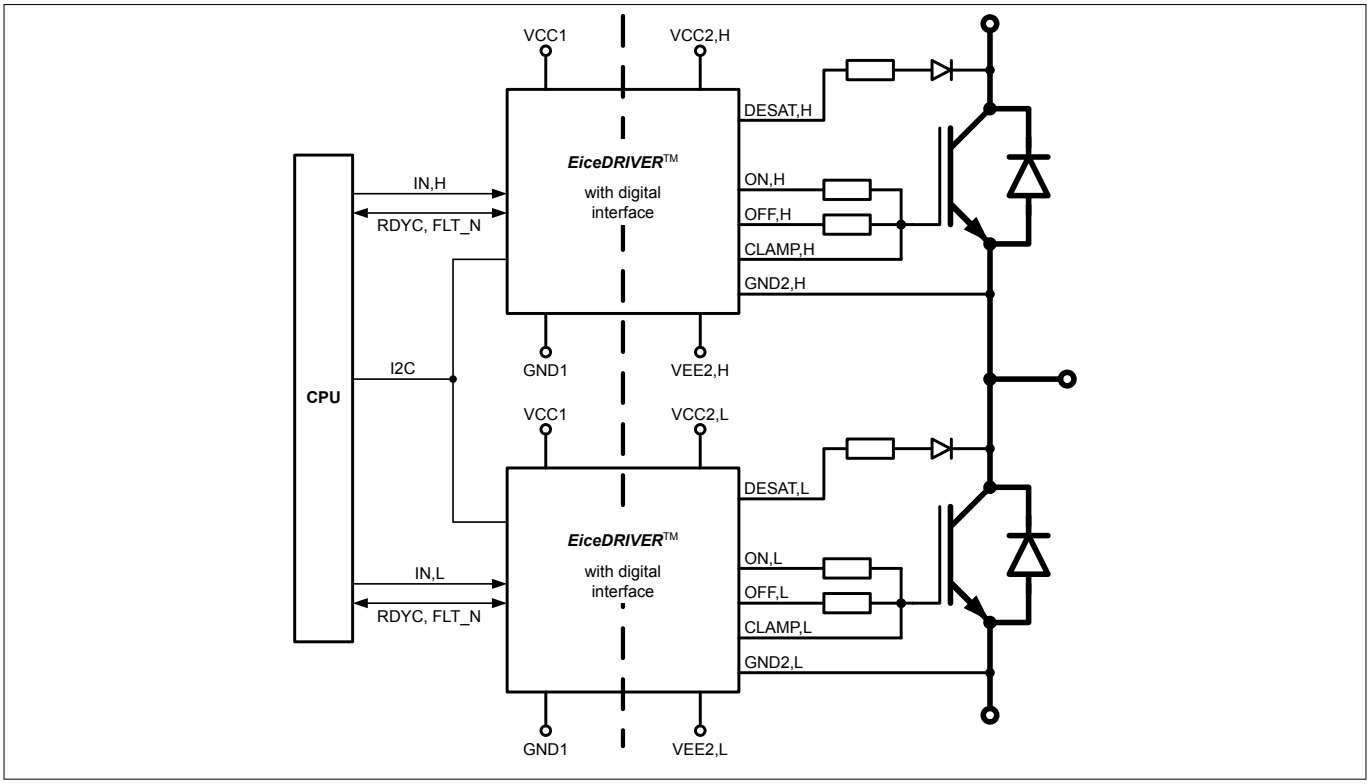

Figure 1 Typical application

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1 Block diagram

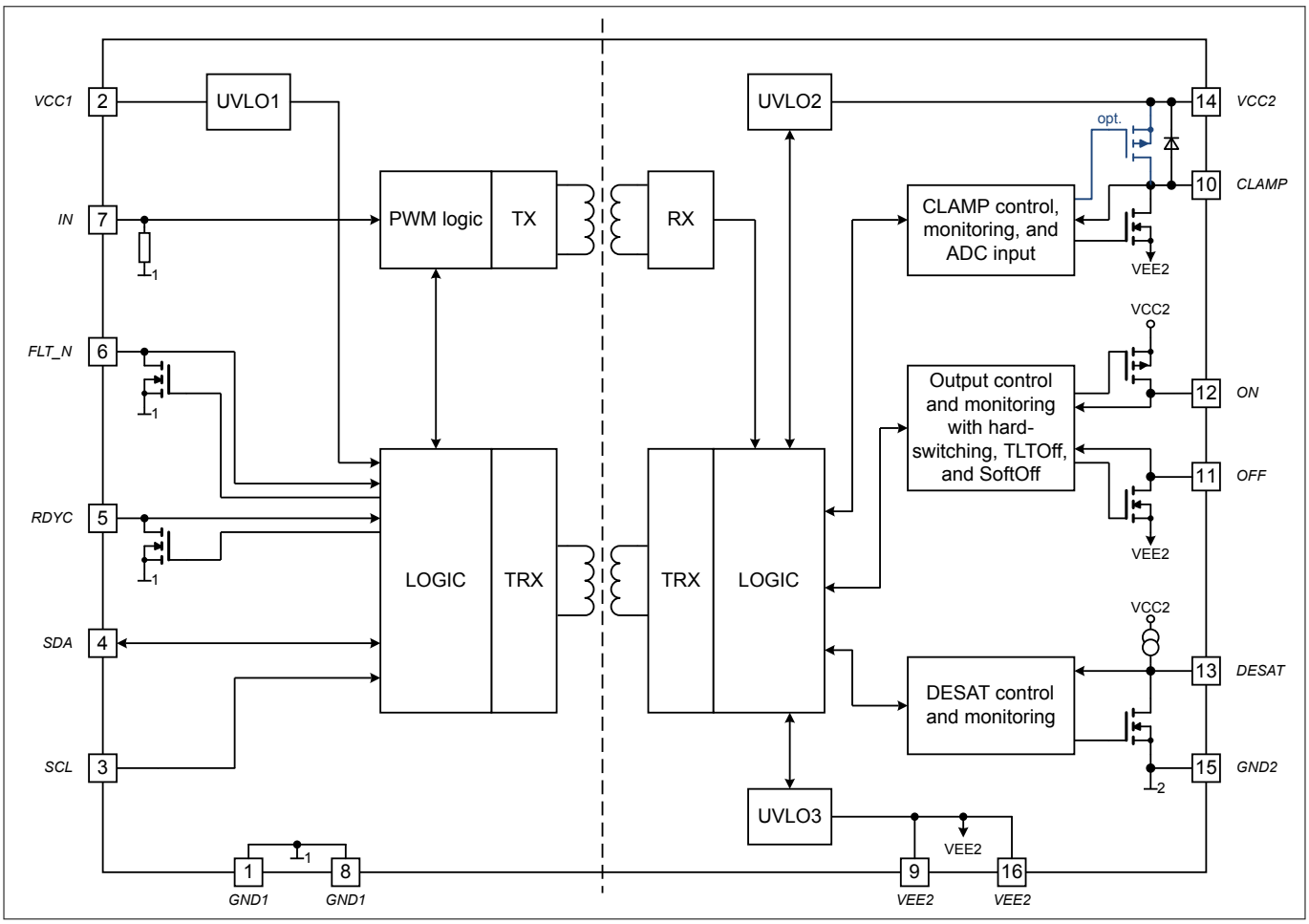


Figure 2 Block diagram

2 Related products

Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	***IKQ75N120CS6***	High Speed 1200 V, 75 A IGBT with anti-parallel diode in TO247-3
	IKW15N120BH6	High Speed 1200 V, 15 A IGBT with anti-parallel diode in TO247
	IHW40N120R5	Reverse conducting 1200 V, 40 A IH IGBT with integrated diode in TO247
CoolSiC™ SiC MOSFET Discrete	***IMBF170R650M1***	1700 V, 650 mΩ SiC MOSFET in TO263-7 package
	IMW120R045M1	1200 V, 45 mΩ SiC MOSFET in TO247-3 package
	IMZ120R350M1H	1200 V, 350 mΩ SiC MOSFET in TO247-4 package
	IMZA65R027M1H	650 V, 27 mΩ SiC MOSFET in TO247-4 package
	IMW65R107M1H	650 V, 107 mΩ SiC MOSFET in TO247-3 package
CoolSiC™ SiC MOSFET Module	***FS45MR12W1M1_B11***	EasyPACK™ 1B 1200 V / 45 mΩ sixpack module
	FF6MR12W2M1_B11	EasyDUAL™ 2B 1200 V, 6 mΩ half-bridge module
	F3L11MR12W2M1_B74	EasyPACK™ 2B 1200 V, 11 mΩ 3-Level module in Advanced NPC (ANPC) topology
	F4-23MR12W1M1_B11	EasyPACK™ 1B 1200 V, 23 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	***F4-200R17N3E4***	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FS150R17N3E4	EconoPACK™ 3 1700 V, 150 A sixpack IGBT module
	FF650R17IE4	PrimePACK™ 3 1700 V, 650 A half-bridge dual IGBT module
	FF1000R17IE4	PrimePACK™ 3 1700 V, 1000 A half-bridge dual IGBT module
	FF1200R17IP5	PrimePACK™ 3+ 1700 V, 1200 A dual IGBT module
	FF1500R17IP5	PrimePACK™ 3+ 1700 V, 1500 A dual IGBT module
	FF1500R17IP5R	PrimePACK™ 3 1700 V, 1500 A dual IGBT module
	FF1800R17IP5	PrimePACK™ 3+ 1700 V, 1800 A dual IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

3 Pin configuration and functionality

The pin assignment at the gate driver IC generally differentiates between the input side and the output side.

Table 1 General pin assignment

Pins	Designation
1 to 8	input side, input logic signal side, or low voltage side
9 to 16	output side, driver power side, or high voltage side

For simplicity reasons the driver is described as an IGBT driver. For use with MOSFETs and other power switches simply replace any mentioning of collector and emitter with their corresponding pin names.

3.1 Pin configuration

Table 2 Pin configuration table abbreviations

Abbreviation	Description
Pin type	
PWR	Power supply and gate current output pins
I/O	Digital input and output pin
I	Digital input pin
GND	Ground reference pin
AI	Analog input pin
Buffer type	
OD	Open drain output
CMOS	CMOS compatible input threshold levels
PP	Push/pull output buffer
analog	Analog input buffer
special	Special output/input function, see individual description
Pull device	
PD	Pull-down resistor
CS	Current source

Table 3 Pin configuration

Pin no.	Pin name	Pin type	Buffer type	Pull device	Function
1	*GND1*	GND	–	–	Ground input side
2	*VCC1*	PWR	–	–	Positive power supply input side
3	*SCL*	I	CMOS	–	Clock input of serial I2C bus
4	*SDA*	I/O	OD, CMOS	–	Data I/O of serial I2C bus
5	*RDYC*	I/O	OD, CMOS	–	Combined ready output, high active and fault clear input and soft-off input, low active
6	*FLT_N*	I/O	OD, CMOS	–	Fault output, low active and soft-off input, low active

Table 3 Pin configuration (continued)

Pin no.	Pin name	Pin type	Buffer type	Pull device	Function
7	*IN*	I	CMOS	PD, 40 kΩ	Non inverted driver input
8	*GND1*	GND	–	–	Ground input side
9	*VEE2*	GND	–	–	Negative power supply output side
10	*CLAMP*	PWR, AI	OD, PP, analog	–	Active Miller clamping with open drain to VEE2, clamp driver for external MOSFET, or ADC input
11	*OFF*	PWR, AI	OD	–	Driver sink output
12	*ON*	PWR, AI	OD	–	Driver source output
13	*DESAT*	AI	special	CS, 500 µA	Enhanced desaturation protection
14	*VCC2*	PWR	–	–	Positive power supply output side
15	*GND2*	AI	–	–	Signal ground output side
16	*VEE2*	GND	–	–	Negative power supply output side

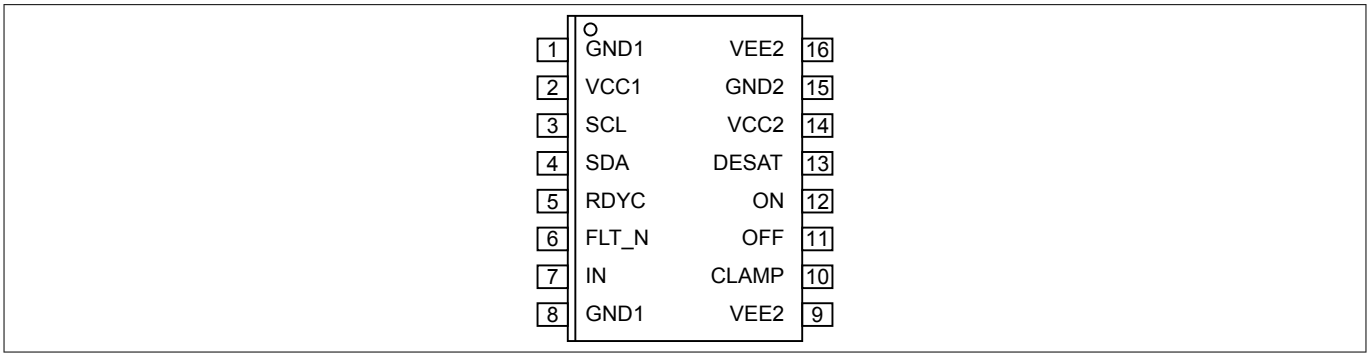


Figure 3 PG-DSO-16 (top view)

3.2 Pin functionality

GND1

Reference ground of the input side. Connect direct to input signal ground.

VCC1

Positive power supply terminal of the input side, connect to 5 V or 3.3 V for proper operation. Place a decoupling capacitor close to this pin and *GND1*.

***SCL* and *SDA* serial bus connection**

Serial data I/O and clock input pin of the I2C bus. Connect to a microcontroller with 5 V or 3.3 V I/O and add a pull-up resistor to positive supply voltage *VCC1*. Signals *SCL* and *SDA* are referenced to *GND1*.

***RDYC* ready status output, fault-off input and fault-clear input**

Open-drain output reports the correct operation of the device, ready output is high active. Fault-clear input and fault-off input clears a gate driver fault or switch the gate driver output to off with fault-off function, input is low active. Connect to a microcontroller with 5 V or 3.3 V I/O with an external pull-up resistor to *VCC1*. A typical value for this resistor is 2.2 kΩ. The *RDCY* signal is referenced to *GND1*.

FLT_N fault output and fault-off input

Open-drain output reports the failures related to operating of the inverter system to the microcontroller, fault output is active low. Fault-off input switch the gate driver output to off with fault-off function, input is low active. Connect to a microcontroller with 5 V or 3.3 V I/O with an external pull-up resistor to *VCC1*. A typical value for this resistor is 2.2 kΩ. The *FLT_N* signal is referenced to *GND1*.

IN non inverting gate driver input

IN input controls the output of the gate driver IC, the IGBT is turned on if *IN* is set to high. Connect to a PWM output of the microcontroller with 5 V or 3.3 V IO. An internal pull-down resistor ensures IGBT off-state if not connected.

VEE2

Negative power supply terminal of the output side. Connect to a voltage of 0 V to -25 V referenced to *GND2* for proper operation. Place a decoupling capacitor close to the following pins:

- *VCC2* and *VEE2*
- *GND2* and *VEE2*

If no negative supply voltage is used, all *VEE2* pins have to be connected to *GND2*.

CLAMP Miller clamp output, Miller clamp pre-driver output, ADC input

The function and operating mode of this pin is depending on the register configuration.

High-current clamp output to hold the gate voltage low during collector-emitter-voltage rise. Connect directly to the gate of the IGBT.

Clamp pre-driver output for the use of an external clamp switch. Connect directly to the gate of a n-channel MOSFET.

Sensing input for 8-bit ADC. Connect the external signal source between *CLAMP* and *VEE2*.

OFF driver output

High-current driver sink output to discharge the gate of the external IGBT and the optional two-level turn-off control output.The gate driver IC also sinks the Soft-off current at this pin. The pin is used as sense input for the gate high-level indicator **PINSTAT**.OFF_PIN and TLTOff comparator **PINSTAT** .TLTO_LVL. Connect to the gate of the IGBT via a chosen turn-off gate resistor.

ON driver output

High-current driver source output to charge the gate of the external IGBT and turn it on and sense input for the CLAMP function. It is also the sense input for the gate low-level indicator **PINSTAT**.ON_PIN. Connect to the gate of the IGBT via a chosen turn-on gate resistor.

DESAT enhanced desaturation detection input

Desaturation detection input to monitor the IGBT collector-emitter voltage (V_{CE}) to detect desaturation caused by short circuit events. Connect to the collector of the driven IGBT via a series connection of a protection resistor and a high-voltage diode. The *DESAT* signal is referenced to *GND2*.

VCC2

Positive power supply terminal of the output side. Connect to sufficient supply voltage referenced to *GND2* for proper operation. Place a decoupling capacitor close to the following pins:

- *VCC2* and *VEE2*
- *VCC2* and *GND2*

GND2 reference ground

Reference ground of the output side. Connect to common voltage of a bipolar supply and the emitter of the IGBT. Place a decoupling capacitor close to the following pins:

- *VCC2* and *GND2*
- *GND2* and *VEE2*

3.3 Configurable parameters via I2C

The following parameters are fully configurable via the I2C interface. The default behavior describes the gate driver configuration if only the address configuration has been set before writing **CFGOK**.USER_OK to 1_B.

Table 4 Configurability via I2C

	Adjustable parameter	Default behavior/value
UVLO	*VCC2-GND2* turn-on UVLO (max)	12.6 V
	VEE2-GND2 UVLO (n.a./-3.5/-6/-12.0 V)	Not active
Output drive	*CLAMP* pin mode (3 A, pre-driver, or ADC)	3 A sink only
	Filter time for CLAMP and pin status monitoring	235 ns
	CLAMP and switch on filter type	Up-reset
	Two-level turn-off	Hard switch-off A = 30 V/ns; 9.0 V; 2.0 µs; B = hard switch-off
	Soft-off current (set as default fault-off method)	**CSSOFCFG**.CSSOFF_I=9_D, 1ED3830M: 146 mA, 1ED3860M: 291 mA, 1ED3890M: 437 mA
	Driver input filter length	103 ns
DESAT	DESAT1 threshold voltage	9.18 V
	Leading edge blanking time	400 ns
	DESAT1 filter time	225 ns
	DESAT1 filter type	Up-reset
	DESAT2 threshold, filter, and action configuration	Disabled
Fault/fault clear	Fault clear source (RDYC or self clear time)	RDYC
	Self clear time (not active, 400 µs, 1600 µs)	Not active
	Fault-off mode (hard switch-off, soft-off, TLTOff)	Hard switch-off
	Over-temperature warning action (warning or fault off)	Warning
	Over-temperature warning level	140°C

4 Functional description

The 1ED38x0Mc12M family (X3 Digital) consists of galvanically isolated single channel gate driver ICs with an extensive digital adjustable feature parameter set. All adjustments are done from low voltage input side during start up via I2C bus. The configuration is stored into registers.

To start-up the gate driver IC for normal operation both input and output sides of the gate driver IC need to be powered.

The 1ED38x0Mc12M family (X3 Digital) is designed to support various supply configurations on the input and output side. On the output side unipolar and bipolar supply is possible.

The output stage is realized as rail-to-rail. There the gate driver voltage follows the supply voltage without an additional voltage drop. In addition it provides an easy clamping of the gate voltage during short circuit of an external IGBT.

The *RDYC* status output reports correct operation of the gate driver IC like sufficient voltage supply. The *FLT_N* status output reports failures in the application like desaturation detection.

To ensure safe operation the gate driver IC is equipped with an input and output side under-voltage lockout circuit. The UVLO levels are optimized for IGBTs and MOSFETs, and are adjustable.

The desaturation detection circuit protects the external IGBT from destruction at a short circuit. The gate driver IC reacts on a DESAT fault by turning off the IGBT with one of the following configurable turn-off methods:

- two-level turn-off
- adjustable soft-off
- hard switch-off

The two-level turn-off (TLTOff) is a voltage controlled turn-off function.

The soft turn-off function is used to switch-off the external IGBT in overcurrent conditions in a soft-controlled manner to protect the IGBT against collector emitter over-voltages.

An adjustable active Miller clamp function protects the IGBT from parasitic turn-on in fast switching applications.

The 1ED38x0 family also offers several measurement and monitoring functions. The monitoring functions can be divided into:

- hardware based functions and
- ADC measurement based functions.

Note: Please refer to the reference manual of this product for a detailed functional description. This chapter does not provide all the information required to fully operate the product.

4.1 Start-up and fault clearing

For normal operation both input and output sides of the gate driver IC need to be powered. A low level at the *FLT_N* pin always indicates a fault condition. In this case the IC starts internal mechanisms for fault clearing.

Input side start-up

1. Voltage at *VCC1* reaches the input UVLO threshold: input side of gate driver IC starts operating
2. *FLT_N* follows input supply voltage
3. Input side is ready to communicate across I2C bus, awaiting user gate driver parameter configuration
4. Records parameters received across the I2C bus
5. Waits until output side is powered
6. Initiates internal start-up: Transfers configured values to output side
7. Performs internal self-test

The complete start-up time t_{START1} depends on the duration of the user parameter configuration.

Output side start-up

1. Voltage at *VCC2* reaches the output UVLO threshold: output side of gate driver IC starts operating
2. Activates OFF gate driver output: connected gate stays discharged
3. Waits until input side is powered
4. Initiates internal start-up: Receives configured values from input side
5. Performs internal self-test

The complete start-up time t_{START2} depends on the duration of the user parameter configuration.

The gate driver IC releases *RDYC* to high to signal a successful start-up and its readiness to operate. The gate driver IC will follow the status of the *IN* signal.

Clearing a fault with *RDYC* to low cycle

1. Set *IN* to low
2. Set *RDYC* to low for a duration longer than the fault clear time t_{CLRMIN}
3. Release *RDYC* to high
   a. If the source of the fault is no longer present, *FLT_N* is released to high
   b. If another fault source is active, *FLT_N* stays low and the cycle needs to be repeated
4. Continue PWM operation

Clearing a fault by self clear timer

1. Set *IN* to low
2. Self clear timer starts counting
3. Self clear timer reaches self clear time
   a. If the source of the fault is no longer present, *FLT_N* is released to high
   b. If another fault source is active, *FLT_N* stays low and the timer restarts
4. Continue PWM operation

4.2 Supply

The 1ED38x0Mc12M family (X3 Digital) is designed to support various supply configurations. The input side can be used with a 3.3 V or 5 V supply.

The output side requires either an unipolar supply (*VEE2* = *GND2*) or a bipolar supply.

- Individual supply voltages between *VCC2* and *GND2* or *GND2* and *VEE2* shall not exceed 25 V.
- The total supply voltage between *VCC2* and *VEE2* shall not exceed 35 V.

To ensure safe operation of the gate driver IC, it is equipped with an input and output side undervoltage lockout circuit.

Unipolar supply

In unipolar supply configuration the gate driver IC is typically supplied with a positive voltage of 15 V at *VCC2*. *GND2* and *VEE2* are connected together and this common potential is connected to the IGBT emitter.

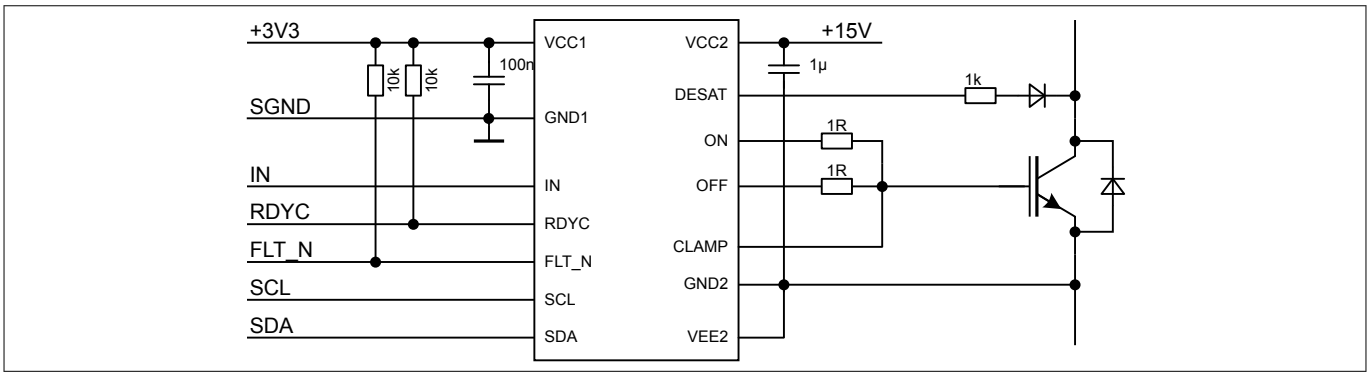


Figure 4 Application example with unipolar supply

Bipolar supply

For bipolar supply the gate driver IC is typically supplied with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V or -15 V at *VEE2* relative to *GND2*.

Between *VCC2* and *VEE2* the maximum potential difference is 35 V.

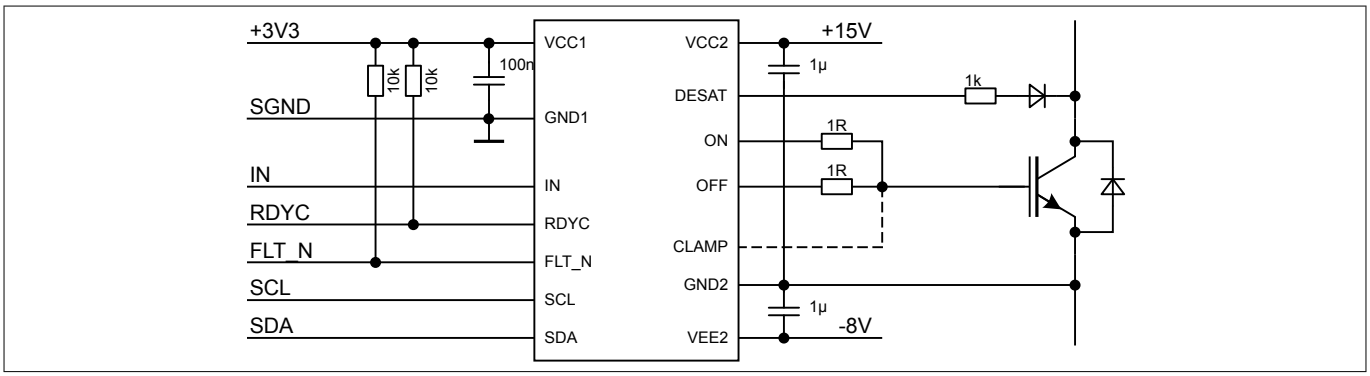


Figure 5 Application example with bipolar supply

Negative supply prevents a parasitic turn-on due to the additional voltage margin to the gate turn-on threshold.

VEE2 over GND2 supply connection check

The gate driver IC has a built-in connection check for *VEE2*. A loss of *VEE2* connection will be detected and signaled via *RDYC*.

4.3 Input side logic

The input threshold levels are always CMOS compliant. The threshold levels are 30% of *VCC1* for low level and 70% of *VCC1* for high level.

The pins *IN* and *SCL* are for input only, and the pins *SDA*, *FLT_N*, and *RDYC* are input/output pins.

4.4 I2C bus

The 1ED38x0 family is equipped with a standard I2C bus interface to configure various parameters of the gate driver IC and read out measurement and monitoring registers.

Key I2C features include:

- I2C bus slave device implementing all mandatory slave bus protocols for the specification ***UM10204 rev. 6***
- 7 bit device addresses for individual and group addressing
- Initial I2C device address: $1A_H$ (MSB aligned, bits 7:1)

4 Functional description

- Signal voltage level compatible to 3.3 V and 5 V
- Supported bus speeds at gate driver data pin (*SDA*) and clock pin (*SCL*):
  - standard-mode (Sm), with bit rates up to 100 kbit/s
  - fast-mode (Fm), with bit rates up to 400 kbit/s
  - fast-mode plus (FM+), with bit rates up to 1 Mbit/s

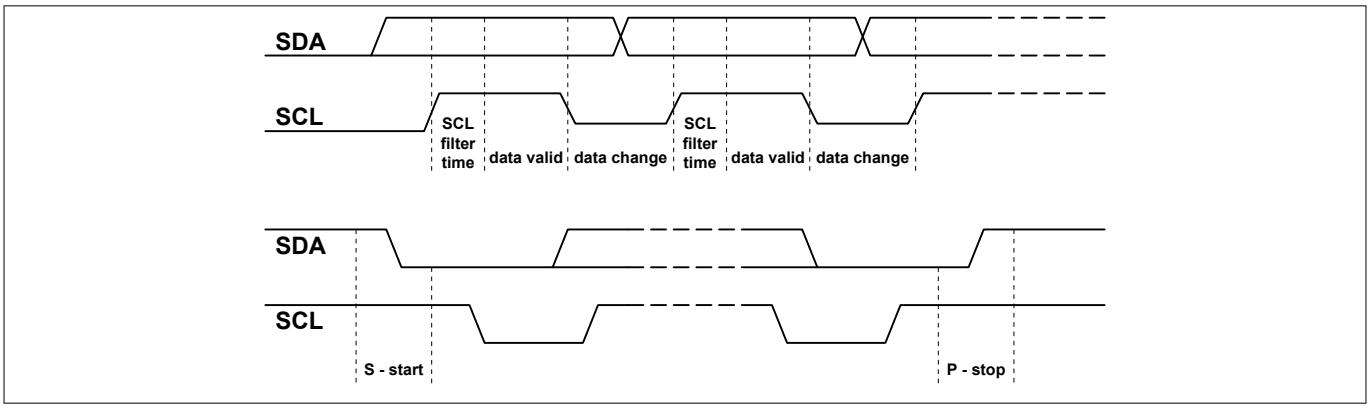


Figure 6 Start, stop and data conditions

All I2C bus commands start with a start condition and stops with a stop condition. The data at the *SDA* pin gets valid if *SCL* level is above the CMOS level threshold and the filter time has elapsed.

4.5 Operating states

The 1ED38x0 family of gate driver ICs can take the following states:

- OFF state, device not powered
- Address configuration state, the I2C addresses can be set, gate driver IC is not active
- Parameter configuration state, the gate driver parameters can be set and changed, gate driver IC is not active
- Parameter transfer state, the gate driver IC is transferring the parameters from input side to output side, gate driver IC is not active
- Normal operation, gate driver IC is active, ON and OFF outputs are following the IN signal, registers are read only
- Not ready state, gate driver IC is switched off according to fault off settings, status signaled by a low at *RDYC* pin
- Fault state, gate driver IC is switched off according to fault off settings, status signaled by a low at *FLT_N* pin
- See later section for additional sub states on fault clear, soft-reset, recover, and restore of parameter configuration after power loss

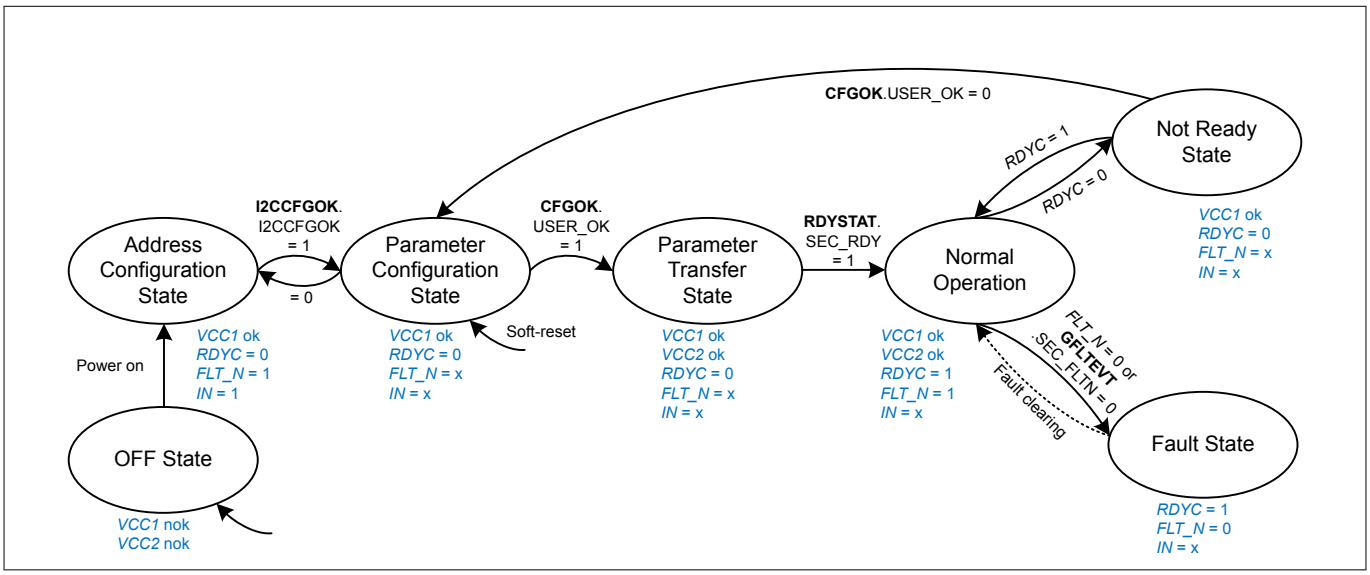


Figure 7 Operating state diagram

- Pin names in uppercase italic letters, supply pin status listed as either okay (ok) or not okay (nok) and for logic pins with low (0), high (1), or either (x)
- Register names in uppercase bold letters followed by the register bit name and value
- States in bubbles with transitions marked by arrows with conditions attached

4.6 Measurement

The 1ED38x0 family offers several measurement functions and uses a free running successive-approximation-register analog-to-digital converter (SAR-ADC). The SAR-ADC has a 8 bit resolution and the results are digitally filtered with a three-point-two pass moving average filter.

Following internal and external parameter measurements are available:

- **ADCMVCC2** Measurement *VCC2* to *VEE2*
- **ADCMVDIF** Measurement and calculation *VCC2* to *GND2*
- **ADCMGND2** Measurement *GND2* to *VEE2*

- **ADCMTEMP** Measurement junction temperature T_J
- **ADCMVEXT** Measurement external voltages, e.g. NTC

Measurement result registers will be updated sequentially depending on selected sample sources. The update rate is typically below 100 µs.

The SAR-ADC configuration register **ADCCFG** is used to activate measurement channels and external voltage compare behavior. Measurement of internal junction temperature is always active. Activated SAR-ADC measurements also enable monitoring functions.

4.7 Monitoring

The 1ED38x0 family offers many monitoring functions. The monitoring functions can be divided into:

- Hardware based functions

  The hardware based monitoring functions use dedicated hardware, e.g. fast UVLO.
- ADC-based functions

  The ADC-based functions gather measured values of different parameters and compare them with limit values. Enable ADC measurement to use related ADC-based monitoring functions.

Both groups contain non-configurable and configurable functions.

Non-configurable hardware monitoring:

- *VEE2* over *GND2*, e.g. *VEE2* connection failure
- Turn-off monitoring, V_{ON} > VEE2+2 V (**FLTEVT**.VOUT_ST = 1_B)
- Gate voltage monitoring below VEE2+2 V (**PINSTAT**.ON_PIN = 1_B)
- Gate voltage monitoring above VCC2-2 V (**PINSTAT**.OFF_PIN = 1_B)
- Gate voltage monitoring above V_{TLTOFF} (**PINSTAT**.TLTO_LVL = 1_B)
- Pin status monitoring of *IN* pin high (**PINSTAT**.PWM_IN = 1_B)
- Pin status monitoring of *RDYC* pin high (**PINSTAT**.RDYC = 1_B)
- Pin status monitoring of *FLT_N* pin high (**PINSTAT**.FLT_N = 1_B)
- *VCC1* supply voltage UVLO spike detection (**UV1FCNT**)
- *VCC2* supply voltage UVLO spike detection (**UV2FCNT**)

Configurable hardware monitoring:

- Normal *VCC2* supply UVLO event (**SECUVEVT**.UV_VCC2)
- Normal *VEE2* supply UVLO event (**SECUVEVT**.UV_VEE2)
- Switch-off timeout, V_{ON} > VEE2+2 V and maximal switch-off timeout time elapsed (**FLTEVT**.SOTO_EVT)

Non-configurable ADC-based monitoring:

- Over temperature protection event (**FLTEVT**.OTP_EVT)

Configurable ADC-based monitoring:

- VCC2 supply soft UVLO event (**SECUVEVT**.UVSVCC2)
- VEE2 supply soft UVLO event (**SECUVEVT**.UVSVEE2)
- External voltage compare event (**FLTEVT**.VEXTFLT)
- Over temperature warning event (**FLTEVT**.OTW_EVT)

Gate driver reaction to *VEE2* over *GND2* detected

A *VEE2* over *GND2* event triggers the following sequence:

1. IC detects *VEE2* over *GND2*
2. IC initiates an output side reset, including
   - Activation of active shutdown as a safety measure

- Resetting all configuration registers to their reset values
- Ignoring all PWM signals and reporting a not ready state

3. IC listens to its previously configured I2C address
- If **RECOVER**.RESTORE = 1_B, the gate driver IC will restore the output side configuration from the input side
- If **RECOVER**.RESTORE = 0_B, the gate driver IC performs a soft-reset and waits for a re-configuration via I2C bus

4. After the configuration of the output side is valid again, the IC continues operation

Note: To avoid unintended VEE2 over GND2 detection, take extra care in power supply design, routing, and capacitive blocking at these pins.

4.8 Desaturation protection

The desaturation detection circuit protects the external IGBT from destruction at a short circuit. The desaturation protection follows the given sequence:

1. Voltage at *DESAT* pin reaches DESAT threshold level, e.g. 9.18 V, for a period of time exceeding the filter time
2. Gate driver IC output switches the external IGBT off, using the defined fault off method
3. Gate driver IC switches *FLT_N* pin to low to indicate the fault to a connected microcontroller
4. Short circuit situation is resolved
   - after the voltage at the *ON* pin has dropped below the *VEE2*+2 V threshold,
   - no other fault condition is present,
   - the input has been turned off and
   - the fault has been cleared using the defined fault clear method

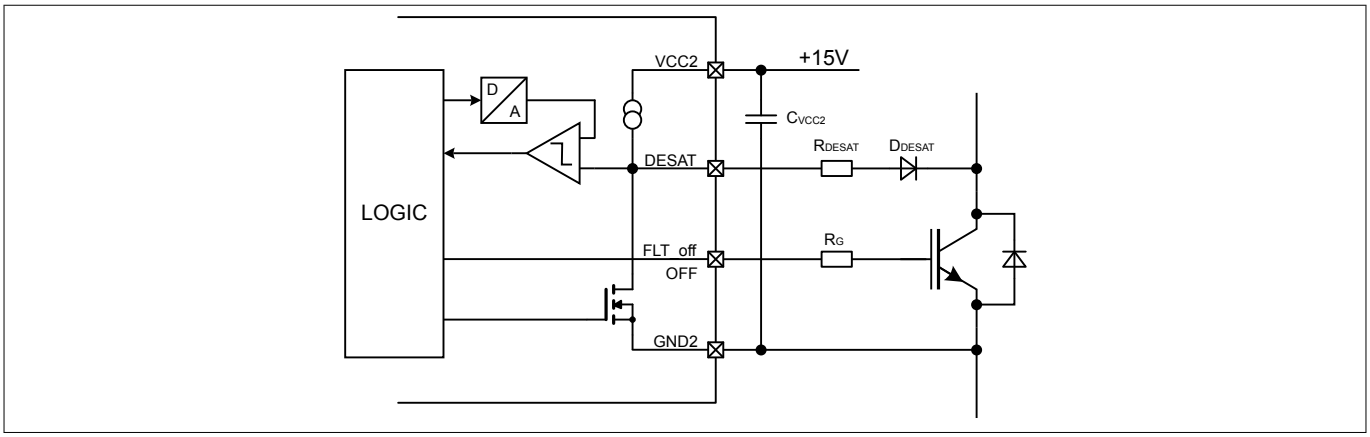


Figure 8 DESAT circuit (only relevant pins shown)

The high-precision internal current source results in a minimum impact on the DESAT detection variation.

4.8.1 DESAT behavior

The DESAT function offers a leading edge blanking time and filters to optimize the DESAT detection for application usage.

The leading edge blanking inhibits threshold detection during an IGBT turn on phase. The typical IGBT turn on behavior starts with charging of the gate, commutation of the application load current and finally V_{CE} voltage decrease to V_{CEsat} voltage levels. To prevent the gate driver IC from detecting a false DESAT event, leading edge blanking pauses the DESAT circuit until the time $t_{DESATleb}$ has elapsed.

Following the leading edge blanking time, the gate driver IC forces the DESAT current into the external DESAT circuit. The current typically flows through a protection resistor, a fast high voltage diode and the collector-emitter path of the IGBT. The resulting voltage at the *DESAT* pin is the sum of the voltage drop across this path.

During a short circuit condition, the V_{CE} voltage increases, resulting in a reverse polarity condition of the DESAT diode. The remaining DESAT current also increases the voltage level at the *DESAT* pin and triggers the DESAT threshold. If the pin voltage level stays above the threshold for the duration of the DESAT filter time $t_{DESATfilter}$, the gate driver IC registers the DESAT event and acts accordingly.

The internal processing time after DESAT threshold crossing, filtering and beginning of fault-off is defined as $t_{DESATOUT}$. The duration of the gate discharge during fault-off is defined as $t_{FLTOFFtot}$ and is depending on the defined fault off function and the gate load.

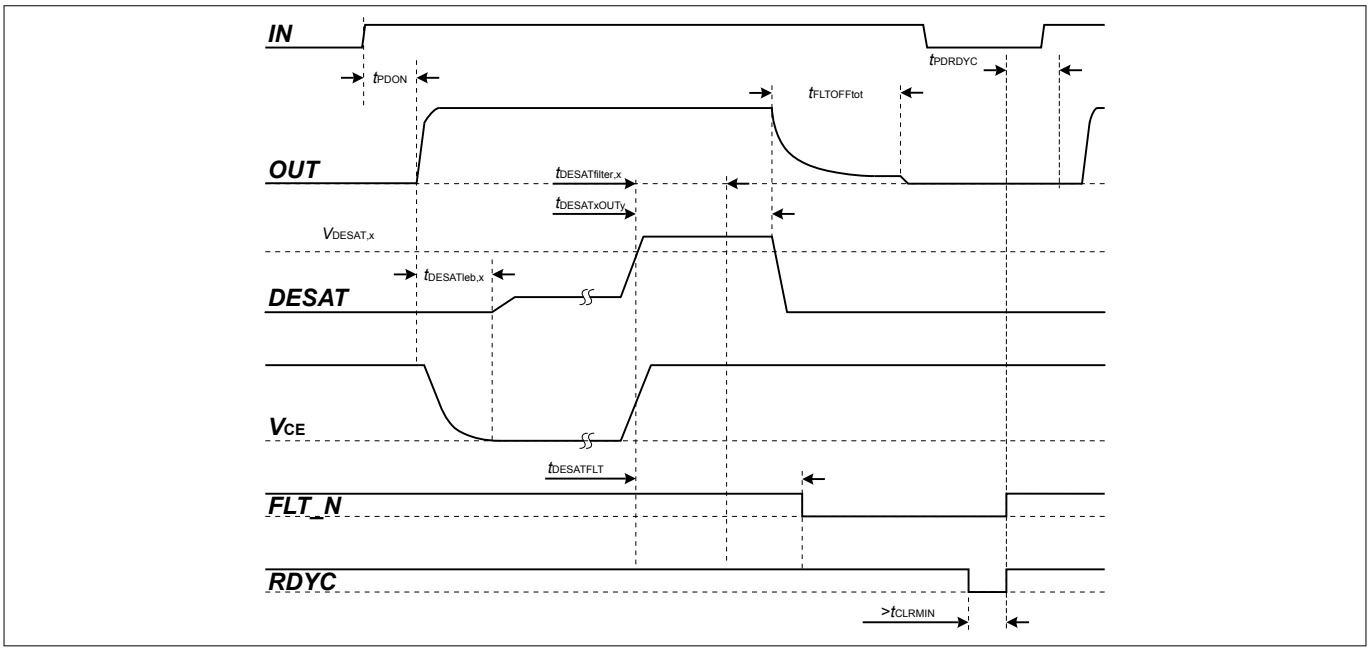


Figure 9 DESAT timing with leading edge blanking, filter and reaction times

4.9 Gate driver output

The gate driver output side uses MOSFETs to provide a rail-to-rail output. Therefore, the gate drive voltage follows the supply voltage closely.

Due to the low internal voltage drop, the switching behavior of the IGBT is predominantly governed by the external gate resistor. The gate driver IC offers separate sink and source outputs to adapt the gate resistor for turn-on and turn-off separately without additional bypass components.

The cell value x in the following table is placeholder for high or low and indicates that this pin does not influence the resulting gate driver output state. The arrow (→) in cells indicate the transition initiated by the pin of the logic input and gate driver supply pins resulting in a transition to the gate driver output state as listed.

Table 5 Driver output state including transition behavior

Logic input and gate driver supply					**Gate driver output**	
IN	***RDYC***	***FLT_N***	***VCC1***	***VCC2***	***ON***	***OFF***
Static gate driver output state: on and off						
high	high	high	high	high	high	tri-state
low	high	high	high	high	tri-state	low
Transition to not ready and static not ready state						
x	high → low	high	high	high	→ tri-state	→ fault off
x	low	high	high	high	tri-state	low
Transition to fault and static fault state						
x	high	high → low	high	high	→ tri-state	→ fault off
x	high	low	high	high	tri-state	low
Transition with VCC1 power loss and unsupplied input side						
x	x	x	high → low	high	→ tri-state	→ fault off
x	x	x	low	high	tri-state	low
Transition with VCC2 power loss and unsupplied output side						
x	x	x	x	high → low	→ tri-state	→ fault off
x	x	x	x	low	tri-state	active shut down

4.9.1 Turn-on behavior

The 1ED38x0Mc12M family (X3 Digital) is optimized for hard switching turn-on. A turn-on command switches the *ON* pin internally to *VCC2*.

4.9.2 Turn-off and fault turn-off behavior

The gate driver IC supports different turn-off sequences to adapt to different applications and IGBT currents during normal switching operation and in the case of a fault.

Table 6 Turn-off sequences

Turn-off reason	Turn-off sequence			Remark
	Hard switching	Two-level turn-off	Soft turn-off	
normal off	X	X		adjustable
fault turn-off	X	X	X	adjustable

The gate driver turn-off behavior can be configured in register **DRVCFG**.STD_OFF.

The gate driver fault turn-off behavior can be configured in register **DRVFOFF**.DRV_FOFF.

In some topologies the fault turn-off needs to be delayed for individual switch positions. The fault turn-off delay time $t_{FAULTOFFn}$ is adjustable in the register **F2ODLY**.F2O_DLY.

The gate driver monitors the gate voltage and sets the register bit **FLTEVT**.VOUT_ST to 1_B as long as the voltage at the *ON* pin is above *VEE2* + 2 V.

Once started, the fault turn-off sequence cannot be interrupted by an *IN* = low turn-off signal.

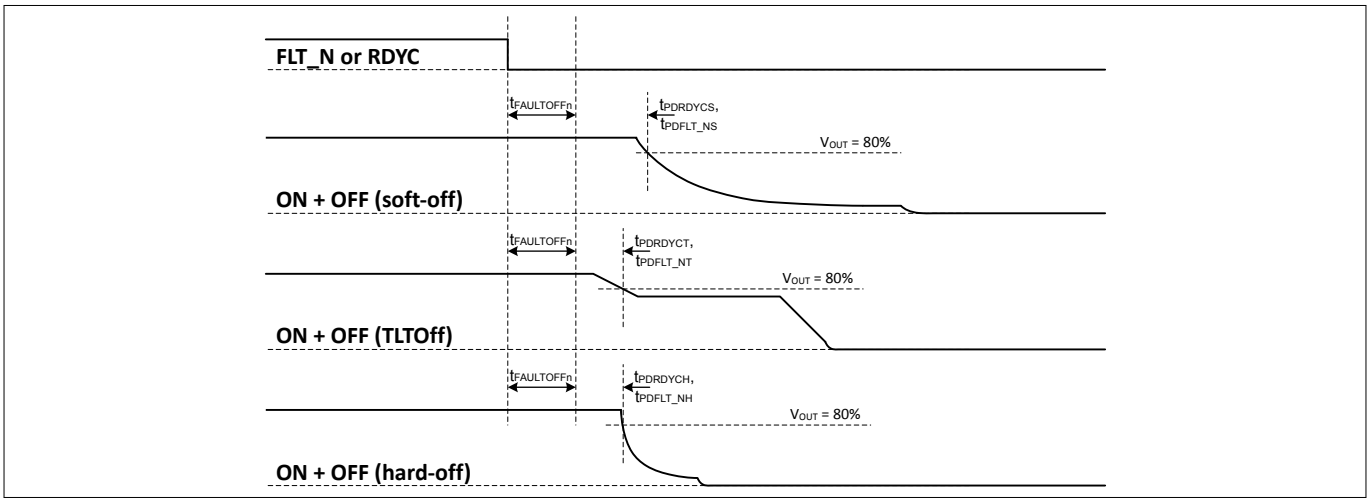


Figure 10 Fault turn-off sequence initiated by *FLT_N* or *RDYC*

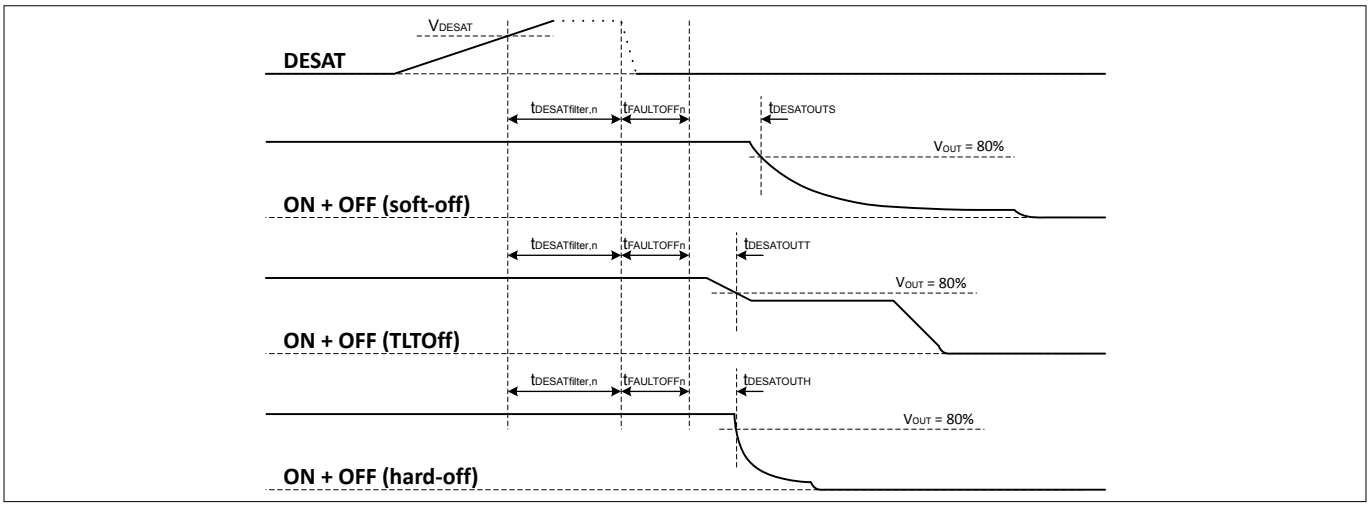


Figure 11 Fault turn-off sequence initiated by DESAT event

4.9.2.1 Hard switching turn-off

Hard switching turn-off supports fast switching applications and applications with emitter-follower booster stages. The switching behavior of the IGBT is controlled by adjusting the external gate resistance between the *OFF* pin and the IGBT gate.

4.9.2.2 Two-level turn-off

The two-level turn-off (TLTOff) is a voltage controlled turn-off function.

Two-level turn-off supports secure IGBT turn-off even under overload conditions with low V_{CE} overshoot. It also operates in applications with emitter-follower booster stages, typical for high power applications with larger d*i*/d*t*. With two-level turn-off the switching behavior of the IGBT is controlled by the plateau voltage and the ramp speed.

The gate driver IC is switching the IGBT gate off by discharging from positive supply to an intermediate voltage level plateau to reduce a collector over current and continued turn-off thereafter. In detail this includes:

1. Discharge gate from *VCC2* voltage level to intermediate voltage level with the controlled voltage ramp A.
2. At the intermediate gate voltage level the IGBT collector current is being limited at overload application conditions.
3. The configured duration of ramp A and intermediate voltage level depends on individual application requirements.
4. Finally the gate voltage is further reduced by the controlled voltage ramp B until the IGBT is completely switched off and the gate voltage reaches *VEE2*.

The gate driver two-level turn-off function can be activated in register**DRVCFG**.STD_OFF. The behavior can be adjusted with four parameters in the registers **TLTOC1** and **TLTOC2**.

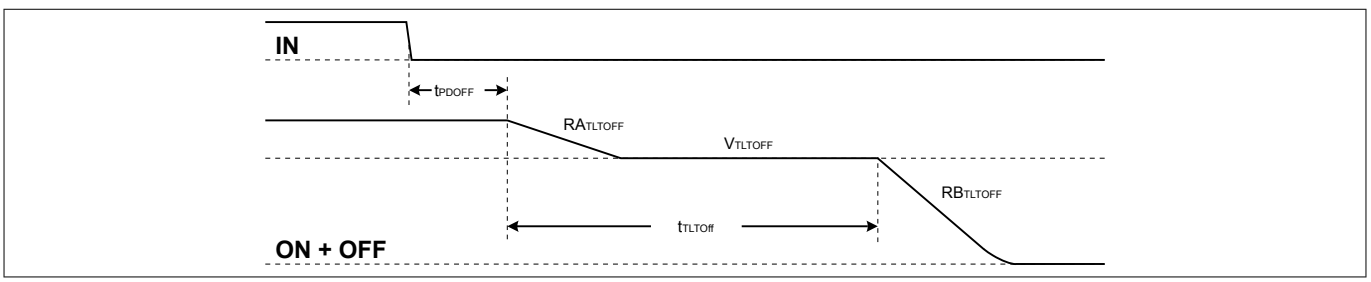


Figure 12 Two-level turn-off timing and ramp-down behavior

In the two-level turn-off mode, the turn-on propagation delay is a function of the plateau time and the gate driver propagation delay without TLTOff function t_{PDon}. This means the gate driver propagation delay will be enlarged by the plateau time for turn-on to ensure a constant on-time of the switch. The two-level turn-off does not change the on-time of an *IN* pulse. The TLTOff voltage will be controlled in a closed loop at the *OFF* output pin of the gate driver IC.

For switch-off initiated by:

- the *IN* signal, the gate driver IC is starting the TLTOff sequence after the propagation delay
- the DESAT function, the gate driver switch-off is delayed by desaturation sense to OFF delay and an optional fault-off delay
- a non-DESAT fault event or a not ready event on output side, the gate driver switch-off occurs immediately or after an optional fault-off delay

After the elapsed plateau time the gate driver IC switches from the plateau voltage down to *VEE2* voltage.

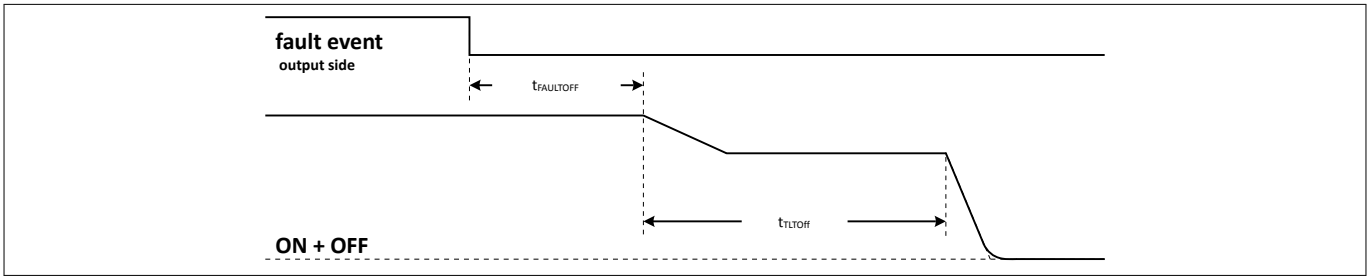


Figure 13 Two-level turn-off after fault event (output side)

For switch-off initiated by:

- *FLT_N* or *RDYC* signal or an internal fault event from input side, the output is switched off after the propagation delay with an optional fault off delay using the defined fault off function

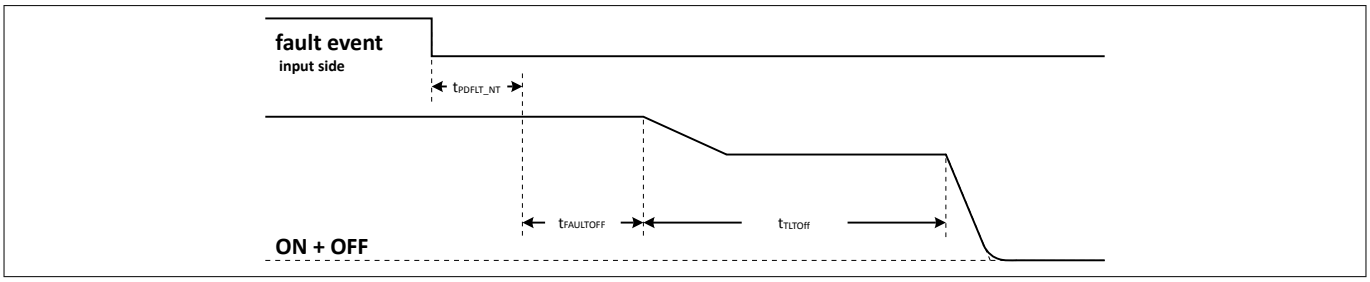


Figure 14 Two-level turn-off after fault event (input side)

4.9.2.3 Soft turn-off

The soft turn-off function protects the IGBT against collector-emitter overvoltage during turn off in an overcurrent condition. It turns-off the IGBT with a reduced gate current to reduce the d*i*/d*t* induced overvoltage..

The IGBT gate is connected via *OFF* to an internal current sink circuit. The discharge current is typically lower than the hard switch-off current used for normal operation. Since soft turn-off is a single event after a failure, the gate driver IC can handle the additional power dissipation internally.

The soft turn-off function is implemented as a current source which can be adjusted with a 4 bit value in the register **CSSOFCFG**.

The adjustable range depends on the current strength of the gate driver IC:

- 1ED3830M: 15 mA - 233 mA
- 1ED3860M: 29 mA - 466 mA
- 1ED3890M: 44 mA - 699 mA

4.9.3 Active shut-down

The active shut-down feature ensures a safe IGBT off-state, if the output chip is not supplied. It protects the IGBT against a floating gate. The IGBT gate is always clamped via *OFF* to *VEE2*.

4.9.4 Active Miller clamp

The 1ED38x0Mc12M family (X3 Digital) is equipped with a configurable active Miller clamp function to protect the IGBT from parasitic turn-on in fast switching applications.

After a turn-off command the gate driver IC follows the implemented sequence:

1. Discharge of the IGBT gate while monitoring the voltage level at the *ON* pin
2. Detection of a voltage at the *ON* pin less than a level of *VEE2* + 2.0 V
3. Filtering of the detection to avoid false CLAMP activation and not to influence regular turn-off behavior
4. Activating clamp function to keep IGBT gate at *VEE2* level

4.10 Short circuit clamping

The integrated short circuit clamping diode limits the IGBT gate over voltage during a short circuit. The over voltage is typically triggered by the capacitive feedback of the Miller capacitance.

The internal diodes from *ON* and *CLAMP* to *VCC2* limit the gate driver voltage to a value slightly higher than the supply voltage. These diode paths are rated for a maximum current of 0.75 A and the duration of 6 µs. Add an external Schottky diode if higher currents are expected or a tighter clamping is desired. Also use an external diode if the active Miller clamping circuit uses the pre-driver output configuration.

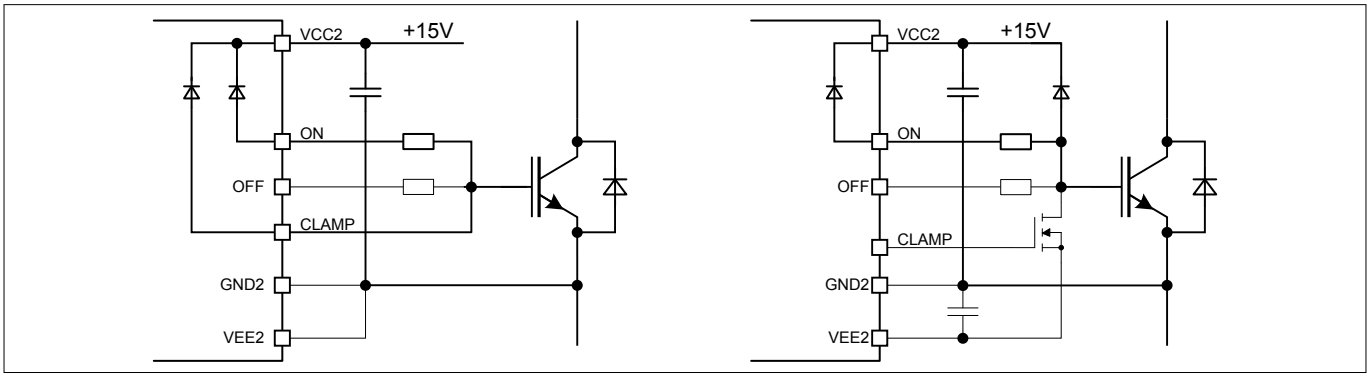


Figure 15 Short circuit clamping circuitry

5 Electrical parameters

5.1 Absolute maximum ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

Table 7 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input to output offset voltage	V_{OFFSET}	–	2300	V	$V_{VEE2,max}$-$V_{VEE2,min}$ with $V_{VEE2,max} \geq V_{GND1} \geq V_{VEE2,min}$ 1) 2)
Supply voltage input side	V_{VCC1}	-0.3	6.5	V	–
Logic input voltage (*IN*)	$V_{LogicIN}$	-0.3	6.5	V	–
Logic input voltage (*RDYC*, *FLT_N*)	$V_{LogicRF}$	-0.3	6.5	V	–
I2C logic input voltage (*SDA*, *SCL*)	$V_{LogicI2C}$	-0.3	6.5	V	–
Open drain logic output current (*RDYC*, *FLT_N*)	$I_{LogicOC}$	–	10	mA	–
I2C logic output current (*SDA*)	I_{SDA}	–	50	mA	–
Positive supply voltage output side	V_{VCC2}	-0.3	40	V	–
Negative supply voltage output side	V_{VEE2}	-40	0.3	V	–
Maximum supply voltage difference output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	40	V	–
DESAT input voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3	V	–
CLAMP input voltage	V_{CLAMP}	V_{VEE2} -0.3	V_{VCC2} +0.3	V	3)
Maximum *CLAMP* output current	I_{CLAMP}	–	2.4	A	$t < 5$ µs
Gate driver output voltage (*ON*, *OFF*)	V_{OUT}	V_{VEE2} -0.3	V_{max2} +0.3	V	–
Maximum *CLAMP* to *VCC2* diode IGBT short circuit clamping time	t_{CLP}	–	6	µs	$I_{CLAMP/OUT}$ = 0.75 A
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_{Stg}	-55	150	°C	–
Power dissipation, input side	$P_{D,IN}$	–	100	mW	@T_A = 25 °C
Power dissipation, output side	$P_{D,OUT}$	–	700	mW	@T_A = 25°C 4)
ESD capability: Human body model	V_{ESDHBM}	–	2	kV	5)
ESD capability: Charged device model	V_{ESDCDM}	–	500	V	6)

1) for functional operation only
2) See also ***Chapter 6*** on page 43
3) May be exceeded during short circuit clamping.

4) Derating the power above 65°C with 8 mW/°C
5) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
6) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

5.2 Thermal parameters

Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

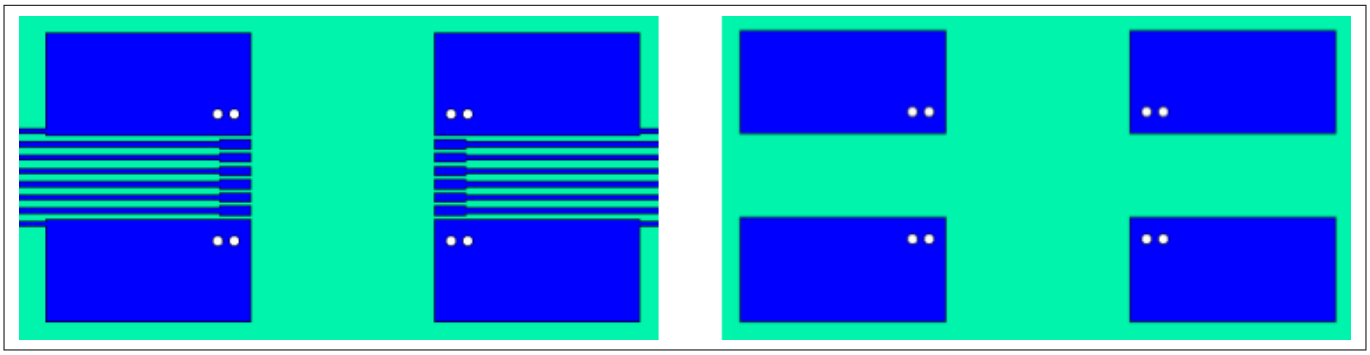


Figure 16 Reference layout for thermal data (Two layer PCB; copper thickness 35 µm; left: top layer; right: bottom layer)

The PCB layout represents the reference layout used for the thermal characterization. Pins 1 and 8 (*GND1*) and pins 9 and 16 (*VEE2*) require ground plane connections for achieving maximum power dissipation. The is conceived to dissipate most of the heat generated through these pins.

Table 8 Thermal parameters

Parameter	Symbol	Value	Unit	Note / Test Condition
Thermal resistance junction to ambient	$R_{THJA,OUT}$	122	K/W	@T_A = 65°C, $P_{D,\ OUT}$ = 400 mW, $P_{D,\ IN}$ = 50 mW, 4 layer test PCB, PG-DSO-16
Characterization parameter junction to package top input side	Ψ_{Jtop}	8	K/W	

5.3 Operating parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

Table 9 Operating parameters

Parameter[1)]	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage input side	V_{VCC1}	3.0	5.5	V	–
Logic input voltages (*IN*, *RDYC*, *FLT_N*, *SDA*, *SCL*)	$V_{LogicIN}$	-0.3	5.5	V	–
Positive supply voltage output side	V_{VCC2}	13	25	V	–

Table 9 Operating parameters (continued)

Parameter[1]	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Negative supply voltage output side	V_{VEE2}	-25	0	V	–
Supply voltage difference output side (V_{VCC2} - V_{VEE2})	V_{max2}	13	35	V	–
Ambient temperature	T_A	-40	125	°C	[2]
Switching frequency	f_{SW}	0	250	kHz	max P_D applies
Common mode transient immunity	$\|CMTI\|$	0	200	V/ns	$V_{OFFSET,test}$ = 1500 V

1) Parameter is not subject to production test - verified by design/characterization
2) T_J has to be below over temperature protection temperature T_{OTPOFF}

5.4 Electrical characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load, and junction temperatures within the operating parameters and default parameter settings unless specified otherwise. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

5.4.1 Voltage supply

Table 10 Voltage supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC1 UVLO threshold	V_{UVLO1H}	–	2.95	3.05	V	–
	V_{UVLO1L}	2.6	2.8	–	V	–
VCC1 UVLO hysteresis (V_{UVLO1H} - V_{UVLO1L})	V_{HYS1}	0.1	0.14	–	V	–
VCC1 quiescent current	I_{Q1}	–	2.4	4.0	mA	V_{VCC1} = 3.3 V, *IN* = High, *RDYC* = High, *FLT_N* = High
VCC1 operating current	I_{O1}	–	2.4	4.0	mA	V_{VCC1} = 3.3 V, *IN* = 16 kHz, 50%, *RDYC* = High, *FLT_N* = High, *SCL* = Low
VCC2 UVLO threshold	$V_{UVLO2H,0}$	–	12.0	12.6	V	**UVTLVL**.UVVCC2TL = 0_H
	$V_{UVLO2L,0}$	10.4	11.0	–	V	
VCC2 UVLO hysteresis ($V_{UVLO2H,0}$ - $V_{UVLO2L,0}$)	$V_{HYS2,0}$	0.75	1.0	–	V	
VCC2 UVLO threshold	$V_{UVLO2H,1}$	–	9.4	10.0	V	**UVTLVL**.UVVCC2TL = 1_H
	$V_{UVLO2L,1}$	8.0	8.7	–	V	
VCC2 UVLO hysteresis ($V_{UVLO2H,1}$ - $V_{UVLO2L,1}$)	$V_{HYS2,1}$	0.6	0.7	–	V	
Soft *VCC2* UVLO voltage level	$V_{UV2S,0}$	–	9.5	–	V	*1)* **UVSVCC2C**.UVSVCC2L
	$V_{UV2S,1}$	–	10.0	–	V	
			...			
	$V_{UV2S,E}$	–	16.5	–	V	
	$V_{UV2S,F}$	–	17.0	–	V	
VEE2 not connected detection threshold	$V_{VEE2,NC}$	–	0.5	–	V	V_{VEE2} - V_{GND2}
VEE2 UVLO threshold	$V_{UVLO3H,1}$	-3.6	-3.5	–	V	**UVTLVL**.UVVEE2TL = 1_H
	$V_{UVLO3L,1}$	–	-3.0	-2.9	V	

Table 10 Voltage supply (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VEE2 UVLO hysteresis ($V_{UVLO3L,1}$ - $V_{UVLO3H,1}$)	$V_{HYS3,1}$	0.4	0.5	–	V	
VEE2 UVLO threshold	$V_{UVLO3H,2}$	-6.15	-6	–	V	**UVTLVL**.UVVEE2TL = 2_H
	$V_{UVLO3L,2}$	–	-5.5	-5.35	V	
VEE2 UVLO hysteresis ($V_{UVLO3L,2}$ - $V_{UVLO3H,2}$)	$V_{HYS3,2}$	0.4	0.5	–	V	
VEE2 UVLO threshold	$V_{UVLO3H,3}$	-12.3	-12.0	–	V	**UVTLVL**.UVVEE2TL = 3_H
	$V_{UVLO3L,3}$	–	-11.0	-10.7	V	
VEE2 UVLO hysteresis ($V_{UVLO3L,3}$ - $V_{UVLO3H,3}$)	$V_{HYS3,3}$	0.8	1.0	–	V	
Soft *VEE2* UVLO voltage level	$V_{UV3S,0}$	–	-2.0	–	V	*1)* **UVSVEE2C**.UVSVCC2E
	$V_{UV3S,1}$	–	-3.0	–	V	
			...			
	$V_{UV3S,E}$	–	-16.0	–	V	
	$V_{UV3S,F}$	–	-17.0	–	V	
VCC2 quiescent current	I_{Q2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = High, *DESAT* = Low, **DRVCFG**.STD_OFF = 0_H, **DRVFOFF** = 00_H/01_H
VCC2 operating current	I_{O2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = 16 kHz, 50%, *DESAT* = Low, C_{LOAD} = 100 pF, **DRVCFG**.STD_OFF = 0_H, **DRVFOFF** = 00_H/01_H

1) Parameter is not subject to production test - verified by design/characterization

5.4.2 Logic input and output

Table 11 Logic input and output

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Logic low input voltage (*IN*, *RDYC*, *FLT_N*, *SDA*, *SCL*)	$V_{LogicINL}$	–	–	30	%	of V_{VCC1}
Logic high input voltage (*IN*, *RDYC*, *FLT_N*, *SDA*, *SCL*)	$V_{LogicINH}$	70	–	–	%	of V_{VCC1}
Logic low output voltage (*RDYC*, *FLT_N*)	V_{RDYC5}, V_{FLT_N5}	–	–	300	mV	I_{SINK} = 5 mA
Logic low output voltage *SDA*	V_{SDA20}	–	–	400	mV	I_{SINK} = 20 mA
Logic input pull down resistor (*IN*)	R_{INPD}	33	40	47	kΩ	–
Logic input pull down resistor (*RDYC*, *FLT_N*)	R_{RDYCPD}, R_{FLT_NPD}	0.8	1.0	1.2	MΩ	–
Logic input current (*SDA*, *SCL*)	I_{SDA}, I_{SCL}	-10	0	+10	µA	0.1**VCC1* < VI < 0.9**VCC1*
Logic input pull down resistor (*SDA*, *SCL*)	R_{SDAPD}, R_{SCLPD}	0.8	1.0	1.2	MΩ	–
Logic pin input capacitance (*SDA*, *SCL*)	C_{SDA}, C_{SCL}	–	–	10	pF	*1)*

1) Parameter is not subject to production test - verified by design/characterization

5.4.3 Gate driver

Note: High and low level output currents are absolute values without an information of current direction.

Table 12 Gate driver

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output voltage	V_{ON0}	–	V_{VCC2} + 0.87	V_{VCC2} + 1.01	V	I_{ON} = 500 mA[1]
High level output peak current 1ED3830M	I_{ON}	2.6	3.8	–	A	[2] [3] C_{LOAD} = 33 nF
High level output on resistance 1ED3830M	$R_{DSON,H}$	0.51	1.12	2.24	Ω	I_{ON} = 67 mA[3]
Low level output peak current 1ED3830M	I_{OFF}	2.0	2.5	–	A	[2] [4] C_{LOAD} = 33 nF
Low level ouput on resistance 1ED3830M	$R_{DSON,L}$	0.31	0.82	1.64	Ω	I_{OFF} = 67 mA[4]
High level output peak current 1ED3860M	I_{ON}	5.2	7.5	–	A	[2] [3] C_{LOAD} = 68 nF
High level output on resistance 1ED3860M	$R_{DSON,H}$	0.26	0.56	1.13	Ω	I_{ON} = 133 mA[3]
Low level output peak current 1ED3860M	I_{OFF}	4.0	5.0	–	A	[2] [4] C_{LOAD} = 68 nF
Low level ouput on resistance 1ED3860M	$R_{DSON,L}$	0.16	0.41	0.83	Ω	I_{OFF} = 133 mA[4]
High Level output peak current 1ED3890M	I_{ON}	7.9	11	–	A	[2] [3] C_{LOAD} = 100 nF
High level output on resistance 1ED3890M	$R_{DSON,H}$	0.17	0.38	0.75	Ω	I_{ON} = 200 mA[3]
Low Level output peak current 1ED3890M	I_{OFF}	6.0	7.5	–	A	[2] [4] C_{LOAD} = 100 nF
Low level ouput on resistance 1ED3890M	$R_{DSON,L}$	0.11	0.28	0.55	Ω	I_{OFF} = 200 mA[4]
Active Shut Down Voltage *OFF* 1ED3830M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 67 mA,V_{VCC2} open
Active Shut Down Voltage *OFF* 1ED3860M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 133 mA,V_{VCC2} open
Active Shut Down Voltage *OFF* 1ED3890M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 200 mA,V_{VCC2} open

1) Integrated diode *ON* vs. *VCC2* clamping test
2) Parameter is not subject to production test - verified by design/characterization
3) *IN* = High, *ON* = High; *VCC2-ON* = 15 V; R_G = 0.1 Ω; *VCC2* = 15 V; *VEE2* = -8 V
4) *IN* = Low, *OFF* = Low; *OFF-VEE2* = 15 V; R_G = 0.1 Ω; *VCC2* = 15 V; *VEE2* = -8 V

5) With reference to *VEE2*

5.4.4 Active Miller clamp

Table 13 Active Miller clamp

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level clamp voltage	$V_{CLAMPH0}$	–	V_{VCC2} +1.5	V_{VCC2} +1.63	V	I_{CLAMP} = 500 mA[1) 2)]
	$V_{CLAMPH1}$	–	V_{VCC2} +0.9	V_{VCC2} +1.1	V	I_{CLAMP} = 50 mA[1) 2)]
Clamp-driver high level output voltage	$V_{CLAMPDH1}$	V_{VEE2}+7.5	V_{VEE2}+9.5	V_{VEE2}+11.5	V	I_{CLAMPH} = 5 mA[3)]
	$V_{CLAMPDH2}$	V_{VEE2}+4.5	V_{VEE2}+6.7	–	V	I_{CLAMPH} = 50 mA[3)]
Clamp-driver high level output peak current	I_{CLAMPH}	0.20	0.27	–	A	[4)] *VCC2* = 15 V; *VEE2* = 0 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 1 Ω
Clamp/Clamp-driver output low level current	$I_{CLAMPL,2}$	1.1	1.8	–	A	[4)] *VCC2* = 15 V; *VEE2* = 0 V; V_{CLAMP} = 2 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 0.1 Ω
Clamp/Clamp-driver output low level current	$I_{CLAMPL,5}$	2.2	3.5	–	A	[4)] *VCC2* = 15 V; *VEE2* = 0 V; V_{CLAMP} = 5 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 0.1 Ω
Clamp/Clamp-driver output low level ON resistance	$R_{DSON,CLP}$	0.50	0.85	1.35	Ω	I_{CLAMPL} = 200 mA
Clamp threshold voltage	V_{ON_CLAMP}	1.5	2.0	2.5	V	Related to *VEE2*
Filter time for CLAMP and pin status monitoring	$t_{CLAMPfilter,1}$	90	105	120	ns	**CLCFG**.CLFILT_T
	$t_{CLAMPfilter,2}$	123	145	167	ns	
	$t_{CLAMPfilter,3}$	159	190	221	ns	
	$t_{CLAMPfilter,4}$	195	235	275	ns	
	$t_{CLAMPfilter,5}$	225	275	325	ns	
	$t_{CLAMPfilter,6}$	263	325	387	ns	
	$t_{CLAMPfilter,7}$	296	370	444	ns	
CLAMP reaction time in CLAMP mode	t_{CLAMP_ON}	16 + $t_{CLAMPfilter}$	23 + $t_{CLAMPfilter}$	35 + $t_{CLAMPfilter}$	ns	[4) 5)] C_{LOAD} = 100 pF
CLAMP reaction time in CLAMP driver mode	t_{CLAMPD_ON}	24 + $t_{CLAMPfilter}$	35 + $t_{CLAMPfilter}$	53 + $t_{CLAMPfilter}$	ns	[4) 6)] C_{LOAD} = 100 pF
Switch-off time-out time	$t_{CTT,0}$	–	0.2	–	µs	[4)] **SOTOUT**.SOTOUT_T
	$t_{CTT,1}$	–	0.4	–	µs	
	$t_{CTT,2}$	–	0.6	–	µs	

Table 13 Active Miller clamp (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$t_{CTT,3}$	–	0.8	–	µs	
	$t_{CTT,4}$	–	1.2	–	µs	
	$t_{CTT,5}$	–	1.6	–	µs	
	$t_{CTT,6}$	–	2.4	–	µs	
	$t_{CTT,7}$	–	3.2	–	µs	
Switch-off time-out soft-off offset time	t_{CTSOOS}	–	2.4	–	µs	4) additional time-out delay during soft-off

1) Integrated diode *CLAMP* vs. *VCC2* clamping test
2) only valid for direct clamping: *IN* = High, *OUT* = High
3) only valid for clamp pre-driver output: *IN* = Low, *OUT* = Low
4) Parameter is not subject to production test - verified by design/characterization
5) CLAMP mode reaction time specified with 3.3 kΩ pull-up from *CLAMP* to 3.3 V, from CLAMP threshold until reaching 0.8 V (falling) at *CLAMP* pin
6) CLAMP driver mode reaction time specified from CLAMP threshold until reaching 0.8 V (rising) at *CLAMP(DRV)* pin

5.4.5 Dynamic characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V, V_{VCC2} = 15 V and V_{VEE2} = -8 V, short filter time (**PSUPR**), hard switch off (**DRVCFG**), and CLAMP function activated unless specified otherwise.

Table 14 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input pulse suppression time *IN*	$t_{INMIN,0}$	98	103	108	ns	**PSUPR**.IN_SUPR
	$t_{INMIN,1}$	174	183	192	ns	
Input pulse suppression time *RDYC*/*FLT_N* for enable / fault off	$t_{RDYCMIN,0}$	85	100	115	ns	**PSUPR**.IN_SUPR
	$t_{RDYCMIN,1}$, $t_{FLT\_NMIN,1}$	153	180	207	ns	
Input pulse width *RDYC* for *FLT_N* reset (Fault clear time)	t_{CLRMIN}	–	1.0	1.2	µs	**FCLR**.FCLR_CFG = 0
Fault self clear time for *FLT_N* reset	$t_{FSCLR,0}$	–	400	440	µs	**FCLR**.FCLR_CFG = 1, **FCLR**.FSCLR_T
	$t_{FSCLR,1}$	–	1600	1760	µs	
Input pulse suppression for I2C (*SDA*, *SCL*)	$t_{I2CMIN,0}$	41	50	59	ns	**PSUPR**.IN_SUPR
	$t_{I2CMIN,1}$	74	90	106	ns	
Output fall time for I2C (*SDA*)	$t_{I2CFALL}$	20	–	120	ns	1) *VCC1* = 5 V; $V_{LogicIN}$ = V_{VCC1}*70% ... V_{VCC1}*30%

Table 14 Dynamic characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input *IN* to output propagation delay *ON*	t_{PDON}	226	244	270	ns	C_{LOAD} = 100 pF, V_{IN} = 70%, V_{OUT}=20%, with $t_{INMIN,0}$
Input *IN* to output propagation delay *OFF*	t_{PDOFF}	218	236	262	ns	C_{LOAD} = 100 pF, V_{IN} = 30%, V_{OUT}=80%, with $t_{INMIN,0}$
Input to output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-23	-8	7	ns	C_{LOAD} = 100 pF
Input *IN* to output propagation delay distortion between any devices (t_{PDON}-t_{PDON}) or (t_{PDOFF}-t_{PDOFF})	t_{PDD}	–	–	30	ns	1) same conditions (V_{IN}, V_{VCC1}, V_{VCC2} and V_{VEE2}, C_{LOAD}, T_A, $t_{INMIN,0}$)
State synchronization time between input and output	t_{SSIO}	–	–	13	µs	1)
Input *RDYC* to output on propagation delay	t_{PDRDYC}	447	523	600	ns	C_{LOAD} = 100 pF; *IN* high; V_{RDYC} = 70%, V_{OUT}=20%, with $t_{INMIN,0}$
Input *RDYC* or *FLT_N* to Soft-off output propagation delay	$t_{PDRDYCS}$, t_{PDFLT_NS}	323	361	407	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, with $t_{MINRDYC,0}$, Soft-off function $I_{CSOFF,15}$
Input RDYC or FLT_N to hard switch-off output propagation delay	$t_{PDRDYCH}$, t_{PDFLT_NH}	303	342	384	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, with $t_{MINRDYC,0}$, OFF function
Input RDYC or FLT_N to TLTOff output propagation delay 1ED3830M	$t_{PDRDYCT}$, t_{PDFLT_NT}	330	387	452	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, with $t_{MINRDYC,0}$, TLTOff function, **TLTOC1**.TLTO_RA = 3_H; .TLTO_V = 13_H; **DRVCFG**.TLTO_GCH = 3_H
Input RDYC or FLT_N to TLTOff output propagation delay 1ED3860M	$t_{PDRDYCT}$, t_{PDFLT_NT}	360	417	482	ns	
Input RDYC or FLT_N to TLTOff output propagation delay 1ED3890M	$t_{PDRDYCT}$, t_{PDFLT_NT}	390	447	512	ns	

Table 14 Dynamic characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Fault off event to fault off delay time	$t_{FAULTOFF,00}$	–	0	–	µs	**F2ODLY**.F2O_DLY Step size 0.25 µs, initial step is 12.5 ns longer
	$t_{FAULTOFF,01}$	-5%	0.263	+5%	µs	
	$t_{FAULTOFF,02}$	-5%	0.513	+5%	µs	
			...			
	$t_{FAULTOFF,1E}$	-5%	7.513	+5%	µs	
	$t_{FAULTOFF,1F}$	-5%	7.763	+5%	µs	
Rise time 1ED3830M	t_{RISE}	–	15	30	ns	C_{LOAD} = 1 nF, V_{OUT}: 20% to 80%
Fall time 1ED3830M	t_{FALL}	–	15	30	ns	C_{LOAD} = 1 nF, V_{OUT}: 80% to 20%
Rise time 1ED3860M	t_{RISE}	–	15	30	ns	C_{LOAD} = 2.2 nF, V_{OUT}: 20% to 80%
Fall Time 1ED3860M	t_{FALL}	–	15	30	ns	C_{LOAD} = 2.2 nF, V_{OUT}: 80% to 20%
Rise Time 1ED3890M	t_{RISE}	–	15	30	ns	C_{LOAD} = 3.3 nF, V_{OUT}: 20% to 80%
Fall Time 1ED3890M	t_{FALL}	–	15	30	ns	C_{LOAD} = 3.3 nF, V_{OUT}: 80% to 20%

1) Parameter is not subject to production test - verified by design/characterization

5.4.6 Desaturation protection

All parameters valid for *VCC1* = 5 V, *VCC2* = 15 V, and *VEE2* = 0 V unless specified otherwise.

Table 15 Desaturation protection

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
DESAT charge current	I_{DESATC}	470	500	525	µA	V_{DESAT} = 0 V
DESAT voltage divider resistance	R_{DVD}	259	312.5	366	kΩ	between *DESAT* and *GND2* pins
DESAT clamp and discharge ON resistance	$R_{DSON,D}$	–	7.7	25.0	Ω	I_{DESATD} = 200 mA
DESAT threshold level	$V_{DESAT,1F}$	8.88	9.18	9.48	V	**D1LVL**.D1_V_LVL, **D2LVL**.D2_V_LVL
	$V_{DESAT,1E}$	8.50	8.89	8.99	V	
	$V_{DESAT,1D}$	8.23	8.61	8.70	V	
	$V_{DESAT,1C}$	7.96	8.33	8.70	V	

Table 15 Desaturation protection (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$V_{DESAT,1B}$	7.68	8.05	8.42	V	
	$V_{DESAT,1A}$	7.41	7.77	8.13	V	
	$V_{DESAT,19}$	7.14	7.49	7.84	V	
	$V_{DESAT,18}$	6.86	7.20	7.54	V	
	$V_{DESAT,17}$	6.63	6.96	7.29	V	
	$V_{DESAT,16}$	6.36	6.68	7.00	V	
	$V_{DESAT,15}$	6.08	6.40	6.72	V	
	$V_{DESAT,14}$	5.81	6.12	6.43	V	
	$V_{DESAT,13}$	5.54	5.84	6.14	V	
	$V_{DESAT,12}$	5.26	5.55	5.84	V	
	$V_{DESAT,11}$	4.99	5.27	5.55	V	
	$V_{DESAT,10}$	4.72	4.99	5.26	V	
	$V_{DESAT,0F}$	4.52	4.79	5.06	V	
	$V_{DESAT,0E}$	4.33	4.59	4.85	V	
	$V_{DESAT,0D}$	4.13	4.39	4.65	V	
	$V_{DESAT,0C}$	3.94	4.19	4.44	V	
	$V_{DESAT,0B}$	3.73	3.98	4.23	V	
	$V_{DESAT,0A}$	3.54	3.78	4.02	V	
	$V_{DESAT,09}$	3.35	3.58	3.81	V	
	$V_{DESAT,08}$	3.16	3.38	3.60	V	
	$V_{DESAT,07}$	2.96	3.18	3.40	V	
	$V_{DESAT,06}$	2.77	2.98	3.19	V	
	$V_{DESAT,05}$	2.57	2.78	2.99	V	
	$V_{DESAT,04}$	2.38	2.58	2.78	V	
	$V_{DESAT,03}$	2.17	2.37	2.57	V	
	$V_{DESAT,02}$	2.02	2.21	2.40	V	
	$V_{DESAT,01}$	1.83	2.01	2.19	V	
	$V_{DESAT,00}$	1.67	1.85	2.03	V	
DESAT leading edge blanking time	$t_{DESATleb,00}$	65	100	134	ns	**DLEBT**.D_LEB_T, V_{ON} 20% rising to V_{DESAT} = 1 V, C_{LOAD} = 100 pF, C_{DESAT} = 2 pF, $t_{FAULTOFF,00}$
	$t_{DESATleb,01}$	163	200	237	ns	
	$t_{DESATleb,02}$	211	250	288	ns	
			...			
	$t_{DESATleb,3E}$	3094	3250	3406	ns	

Table 15 Desaturation protection (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$t_{DESATleb,3F}$	3142	3300	3458	ns	
DESAT filter time	$t_{DESATfilter,00}$	–	–	–	ns	**D1FILT**.D1FILT_T, **D2FILT**.D2FILT_T
	$t_{DESATfilter,01}$	48	75	105	ns	
		–	...	–	ns	
	$t_{DESATfilter,06}$	286	325	368	ns	
	$t_{DESATfilter,07}$	333	375	421	ns	
	$t_{DESATfilter,08}$	429	475	526	ns	
			...			
	$t_{DESATfilter,0E}$	1000	1075	1158	ns	
	$t_{DESATfilter,0F}$	1095	1175	1263	ns	
	$t_{DESATfilter,10}$	1286	1375	1474	ns	
			...			
	$t_{DESATfilter,16}$	2429	2575	2737	ns	
	$t_{DESATfilter,17}$	2619	2775	2947	ns	
	$t_{DESATfilter,18}$	3000	3175	3368	ns	
			...			
	$t_{DESATfilter,1E}$	5286	5575	5895	ns	
	$t_{DESATfilter,1F}$	5667	5975	6316	ns	
DESAT1 sense to *FLT_N* low delay	$t_{DESAT1FLT}$	623	743	883	ns	V_{FLT_N} = 30%, I_{FLT_N} = 5 mA, $t_{DESATfilter,04}$, C_{FLT_N} = 100 pF
DESAT2 sense to *FLT_N* low delay	$t_{DESAT2FLT}$	673	793	933	ns	
DESAT1 sense to *OFF* low delay, Soft-off	$t_{DESAT1OUTS}$	287 + $t_{DESATfilter}$	333 + $t_{DESATfilter}$	382 + $t_{DESATfilter}$	ns	V_{OUT} = 80%, C_{LOAD} = 100 pF, $t_{FAULTOFF,n}$ = 0 µs, $I_{CSOFF,15}$
DESAT2 sense to *OFF* low delay, Soft-off	$t_{DESAT2OUTS}$	337 + $t_{DESATfilter}$	383 + $t_{DESATfilter}$	432 + $t_{DESATfilter}$	ns	
DESAT1 sense to *OFF* low delay , TLTOff, 1ED3830M	$t_{DESAT1OUTT3}$	294 + $t_{DESATfilter}$	359 + $t_{DESATfilter}$	427 + $t_{DESATfilter}$	ns	V_{OUT} = 80%, C_{LOAD} = 100 pF, $t_{FAULTOFF,n}$ = 0 µs, **TLTOC1**.TLTO_RA = 3_H, **TLTOC1**.TLTO_V = 13_H, **DRVCFG**.TLTO_GCH = 3_H
DESAT1 sense to *OFF* low delay , TLTOff, 1ED3860M	$t_{DESAT1OUTT6}$	324 + $t_{DESATfilter}$	389 + $t_{DESATfilter}$	457 + $t_{DESATfilter}$	ns	
DESAT1 sense to *OFF* low delay , TLTOff, 1ED3890M	$t_{DESAT1OUTT9}$	354 + $t_{DESATfilter}$	419 + $t_{DESATfilter}$	487 + $t_{DESATfilter}$	ns	

Table 15 Desaturation protection (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
DESAT2 sense to *OFF* low delay , TLTOff, 1ED3830M	$t_{DESAT2OUTT3}$	344 + $t_{DESATfilter}$	409 + $t_{DESATfilter}$	477 + $t_{DESATfilter}$	ns	
DESAT2 sense to *OFF* low delay , TLTOff, 1ED3860M	$t_{DESAT2OUTT6}$	374 + $t_{DESATfilter}$	439 + $t_{DESATfilter}$	507 + $t_{DESATfilter}$	ns	
DESAT2 sense to *OFF* low delay , TLTOff, 1ED3890M	$t_{DESAT2OUTT9}$	404 + $t_{DESATfilter}$	469 + $t_{DESATfilter}$	537 + $t_{DESATfilter}$	ns	
DESAT1 sense to *OFF* low delay, hard switch-off	$t_{DESAT1OUTH}$	267 + $t_{DESATfilter}$	314 + $t_{DESATfilter}$	359 + $t_{DESATfilter}$	ns	V_{OUT} = 80%, C_{LOAD} = 100 pF, $t_{FAULTOFF,n}$ = 0 µs
DESAT2 sense to *OFF* low delay, hard switch-off	$t_{DESAT2OUTH}$	317 + $t_{DESATfilter}$	364 + $t_{DESATfilter}$	409 + $t_{DESATfilter}$	ns	

5.4.7 Two-level turn-off

Table 16 Two-level turn-off

Parameter[1]	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Two-level turn-off time[2]	$t_{TLTOff,00}$	–	0	–	µs	**TLTOC2**.TLTO_T; C_{LOAD} = 100 pF; $t_{MININ,0}$; V_{VCC2} = 15 V; V_{VEE2} = -8 V; V_{VCC1} = 5 V; $RA_{TLTOff,3}$; $RB_{TLTOff,0}$; $V_{TLTOff,13}$
	$t_{TLTOff,01}$	-5%	0.25	+5%	µs	
		–	...	–		
	$t_{TLTOff,1E}$	-5%	7.50	+5%	µs	
	$t_{TLTOff,1F}$	-5%	7.75	+5%	µs	
Two-level turn-off ramp A	$RA_{TLTOff,0}$	–	7.5	–	V/µs	**TLTOC1**.TLTO_RA
	$RA_{TLTOff,1}$	–	15	–	V/µs	
	$RA_{TLTOff,2}$	–	30	–	V/µs	
	$RA_{TLTOff,3}$	–	60	–	V/µs	
Two-level turn-off ramp B	$RB_{TLTOff,4}$	–	7.5	–	V/µs	**TLTOC2**.TLTO_RB
	$RB_{TLTOff,5}$	–	15	–	V/µs	
	$RB_{TLTOff,6}$	–	30	–	V/µs	
	$RB_{TLTOff,7}$	–	60	–	V/µs	
	$RB_{TLTOff,0}$	–	max	–	V/µs	hard switch-off, not controlled, compare to driver fall time
Two-level turn-off plateau voltage	$V_{TLTOff,00}$	–	4.25	–	V	**TLTOC1**.TLTO_V
	$V_{TLTOff,01}$	–	4.5	–	V	
			...			
	$V_{TLTOff,1E}$	–	11.75	–	V	
	$V_{TLTOff,1F}$	–	12.0	–	V	

1) Parameter is not subject to production test - verified by design/characterization
2) Two-level turn-off time defined as: Time from turn-off threshold (V_{IN}=30%) to output off detection threshold (V_{OFF}=V_{VEE2}+2 V) minus turn-off propagation delay t_{PDOFF}

5.4.8 Soft-off current source

Soft-off current source values specified at *OFF* pin at V_{OFF} = 3 V with unipolar supply of V_{VCC2} = 15 V.

Table 17 Current source turn-off

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Soft-off current source current 1ED3830M	$I_{CSOFF,0}$	10	15	19	mA	**CSSOFCFG**.CSSOFF_I
	$I_{CSOFF,1}$	24	29	36	mA	
	$I_{CSOFF,2}$	35	44	52	mA	
	$I_{CSOFF,3}$	47	58	70	mA	
	$I_{CSOFF,4}$	58	73	87	mA	
	I_{CSOFF5}	70	87	105	mA	
	$I_{CSOFF,6}$	82	102	122	mA	
	$I_{CSOFF,7}$	93	116	140	mA	
	$I_{CSOFF,8}$	105	131	157	mA	
	$I_{CSOFF,9}$	116	146	175	mA	
	$I_{CSOFF,10}$	128	160	192	mA	
	$I_{CSOFF,11}$	140	175	210	mA	
	$I_{CSOFF,12}$	151	189	227	mA	
	$I_{CSOFF,13}$	163	204	245	mA	
	$I_{CSOFF,14}$	175	218	262	mA	
	$I_{CSOFF,15}$	186	233	280	mA	
Soft-off current source current 1ED3860M	$I_{CSOFF,0}$	22	29	36	mA	**CSSOFCFG**.CSSOFF_I
	$I_{CSOFF,1}$	45	58	72	mA	
	$I_{CSOFF,2}$	70	87	105	mA	
	$I_{CSOFF,3}$	93	116	140	mA	
	$I_{CSOFF,4}$	116	146	175	mA	
	$I_{CSOFF,5}$	140	175	210	mA	
	$I_{CSOFF,6}$	163	204	245	mA	
	$I_{CSOFF,7}$	186	233	280	mA	
	$I_{CSOFF,8}$	210	262	314	mA	
	$I_{CSOFF,9}$	233	291	349	mA	
	$I_{CSOFF,10}$	256	320	384	mA	
	$I_{CSOFF,11}$	280	349	419	mA	
	$I_{CSOFF,12}$	303	379	454	mA	
	$I_{CSOFF,13}$	326	408	489	mA	
	$I_{CSOFF,14}$	349	437	524	mA	

Table 17 Current source turn-off (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$I_{CSOFF,15}$	373	466	559	mA	
Soft-off current source current 1ED3890M	$I_{CSOFF,0}$	34	44	54	mA	**CSSOFCFG**.CSSOFF_I
	$I_{CSOFF,1}$	70	87	105	mA	
	$I_{CSOFF,2}$	105	131	157	mA	
	$I_{CSOFF,3}$	140	175	210	mA	
	$I_{CSOFF,4}$	175	218	262	mA	
	$I_{CSOFF,5}$	210	262	314	mA	
	$I_{CSOFF,6}$	245	306	367	mA	
	$I_{CSOFF,7}$	280	349	419	mA	
	$I_{CSOFF,8}$	314	393	472	mA	
	$I_{CSOFF,9}$	349	437	524	mA	
	$I_{CSOFF,10}$	384	480	577	mA	
	$I_{CSOFF,11}$	419	524	629	mA	
	$I_{CSOFF,12}$	454	568	681	mA	
	$I_{CSOFF,13}$	489	612	734	mA	
	$I_{CSOFF,14}$	524	655	786	mA	
	$I_{CSOFF,15}$	559	699	839	mA	

5.4.9 Over-temperature protection

Table 18 Over-temperature protection and over-temperature warning

Parameter[1)]	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Over-temperature protection level	T_{OTPOFF}	150	160	170	°C	
Over-temperature warning level	$T_{OTW,7}$	–	95	–	°C	**OTWCFG**.OTW_LVL
	$T_{OTW,6}$	–	101	–	°C	
	$T_{OTW,5}$	–	108	–	°C	
	$T_{OTW,4}$	–	114	–	°C	
	$T_{OTW,3}$	–	120	–	°C	
	$T_{OTW,2}$	–	127	–	°C	
	$T_{OTW,1}$	–	134	–	°C	
	$T_{OTW,0}$	–	140	–	°C	

1) Parameter is not subject to production test - verified by design/characterization

5.4.10 ADC measurement

Table 19 ADC voltage and temperature measurement

Parameter[1)]	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Internal ADC voltage max	$V_{ADCINTmax}$	–	38.67	–	V	**ADCMVCC2**/ **ADCMGND2**/ **ADCMVDIF** = FF_H
Internal ADC voltage resolution	$V_{ADCINTres}$	–	151.5	–	mV	
External ADC voltage max	$V_{ADCEXTmax}$	–	2.86	–	V	**ADCMVEXT** = FF_H
External ADC voltage resolution	$V_{ADCEXTres}$	–	11.2	–	mV	
Internal temperature ADC max	$T_{ADCTEMPmax}$	140	150	160	°C	**ADCMTEMP** = 84_H
Internal temperature ADC min	$T_{ADCTEMPmin}$	–	-40	–	°C	**ADCMTEMP** = 49_H
Internal temperature ADC resolution	$T_{ADCTEMPres}$	–	3.21	–	°C	

1) Parameter is not subject to production test - verified by design/characterization

6 Insulation characteristics

The following isolation classes are available for the 1ED38x0Mc12M family (X3 Digital).

Table 20 Product isolation classes

Product name	Marking	Insulation characteristics	Values specified in	UL values
1ED38x0MU12M	38x0MU12	UL 1577 certified insulation	-	***Table 23***
1ED38x0MC12M	38x0MC12	Reinforced insulation	***Table 22***	***Table 23***

Table 21 Safety limiting values

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Description	Symbol	Characteristic	Unit
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at T_A = 25°C	P_{SI}	100	mW
Maximum output-side power dissipation at T_A = 25°C[1)]	P_{SO}	1000	mW
Maximum driver output current (*ON*, *OFF*)[2)]	I_{OUT}		A
1ED3830MC		2.4	
1ED3860MC		4.8	
1ED3890MC		7.2	

1) IC output-side power dissipation is derated linearly at 8 mW/°C above 65 °C
2) Maximum pulse length of t = 5 µs

6.1 Certified according to VDE 0884-11 reinforced insulation (pending)

Valid for parts with part name 1ED38x0MC12M, x indicate different variants.

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 22 Reinforced insulation according to VDE 0884-11

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1			–
for rated mains voltage ≤ 150 V (rms)		I-IV	
for rated mains voltage ≤ 300 V (rms)		I-IV	
for rated mains voltage ≤ 600 V (rms)		I-III	
for rated mains voltage ≤1000 V (rms)		I-II	
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Minimum external clearance	*CLR*	>8	mm
Minimum external creepage	*CPG*	>8	mm
Minimum comparative tracking index	*CTI*	400	–

Table 22 Reinforced insulation according to VDE 0884-11 (continued)

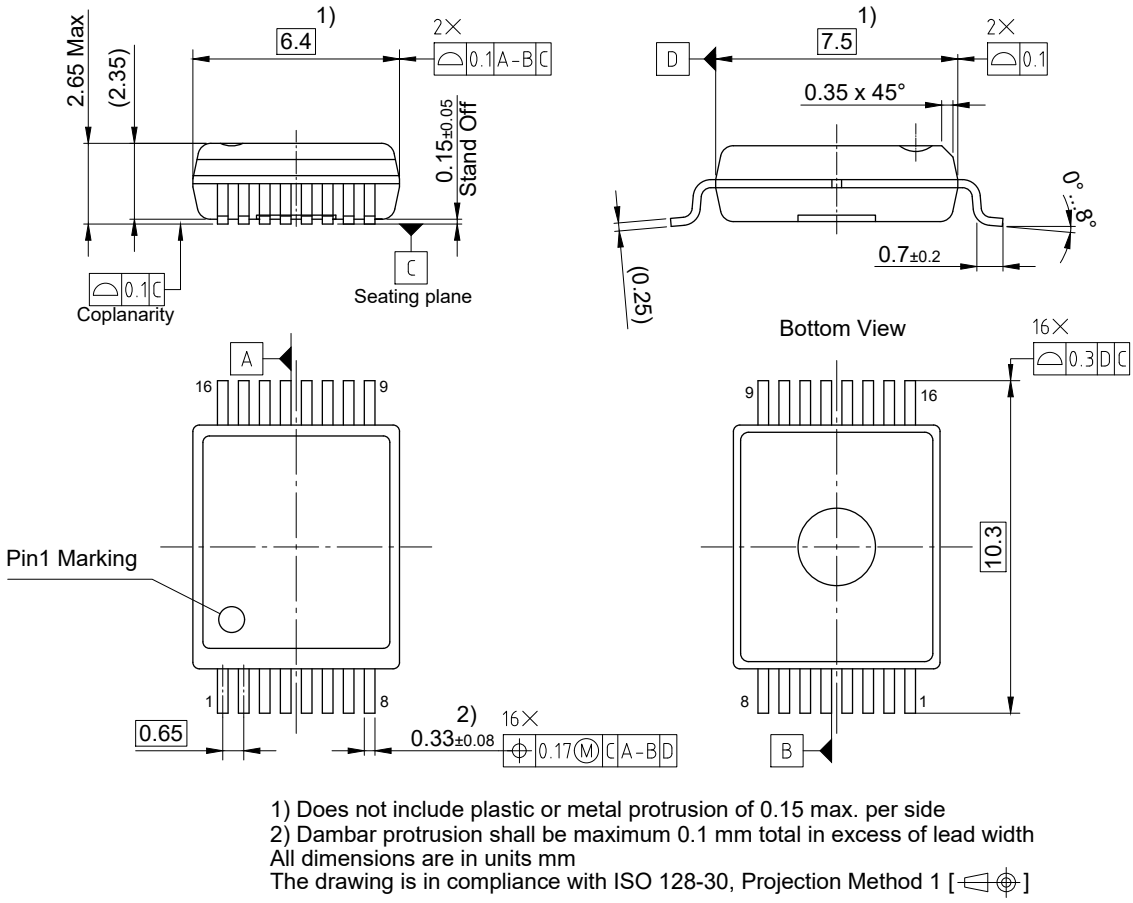
Description	Symbol	Characteristic	Unit
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)}$ = 4500 V, t_{ini} = 1 min	q_C	<5	nC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)}$ = 4500 V, t_{ini} = 1 s	q_C	<5	nC
Isolation resistance at $T_{A,max}$	R_{IO}	> 10^{11}	Ω
Isolation resistance at T_S	R_{IO_S}	> 10^9	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive insulation voltage	V_{IORM}	1767	V (peak)
Maximum surge isolation voltage for reinforced isolation $V_{TEST} = V_{IOSM} \times 1.6$	V_{IOSM}	6875	V (peak)
Insulation capacitance	C_{IO}	1.7	pF

6.2 Recognized under UL 1577 (File E311313)

Table 23 Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation withstand voltage/1 min	V_{ISO}	5700	V (rms)
Insulation test voltage/1 s	$V_{ISO, TEST}$	6840	V (rms)

7 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 17 PG-DSO-16-28/33 - 300 mil 16-pin fine pitch plastic green dual small outline package

Revision history

Revision History	
Reference	**Description**
v2.1	• Change footnotes to tablenotes, added parameter V_{OFFSET} • Product links and certification information update
v2.0	Editorial changes
v1.0	Parameter tables competed, editorial changes in functional description
v0.8	Editorial changes in functional description and parameter tables

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